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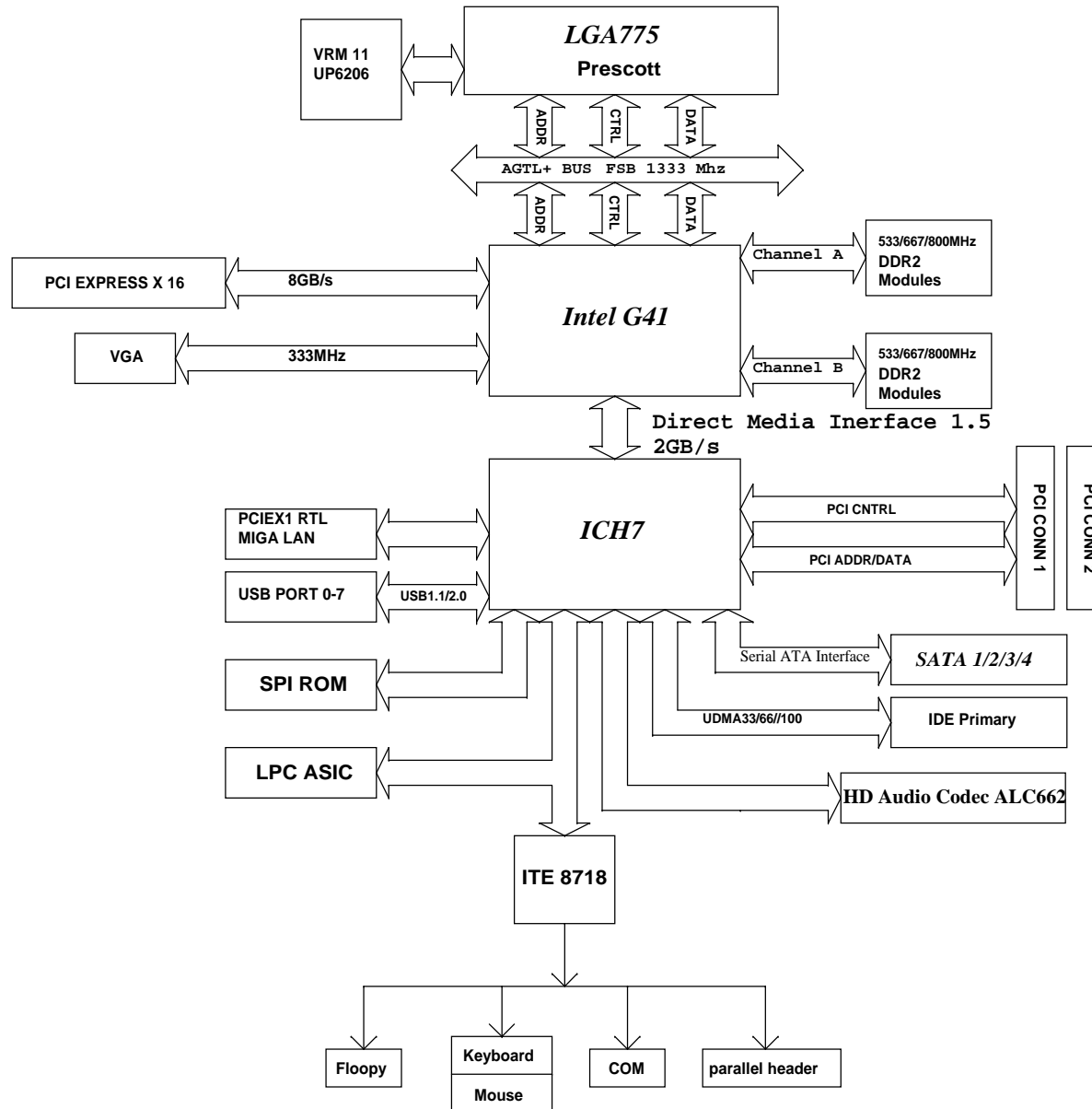
## IG41A-M7S

uATX    VER:6.5

775 CPU , FSB1600 ,  
PCI-Ex16 , DDR-II\* 2  
, 10/100 LAN,PCI\*2

		<b>映泰股份有限公司</b> <b>BIOSSTAR GROUP</b>	
<b>Title</b> <b>Cover Sheet</b>			
<b>Size</b> Custom	<b>Document Number</b> <b>IG41A-M7S</b>		<b>Rev</b> 6.5
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# BLOCK DIAGRAM



PCI Slot	IDE SEL	INT#	GNT#	REQ#	CLOCK
1					
2					

Chips	IDE SEL	INT#	GNT#	REQ#	CLOCK	GPIO
PATA						
ICH7						
S						
I/O BIOS						
LAN						
ANTI-POP						
DIMM-OV						
CPU-OV						
SATA-LED						
S						
I/O						

- 5

4

3

2

1
- V0. 6-->V0. 65
- 1.H\_TESTHI\_7\_2 pull high

2.H\_CPURST#, H\_BR0# pull high, H\_TRST#, H\_TCK pull down

3. 新增FB17, C196, R44改成0805

4.R280 pull down ,add R326 R327 R328 R329

5.IDE RESET change PCI\_RST\_OUT1#

6.add AR23 AR24 APR1

7.add PC38 , PR1=10K->1K, PR17=2. 4K->1. 8K, R315=22K->18K, R316=47K->40. 2K

8.R325 pull high VCC5SB

9.R200=20K->14. 7K, R202=7. 5K->5. 1K


10.R217 pull high 3V3\_DUAL

11.add PRN3 R259, R257=10K->1K
- D

C

B

A



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Change Lise

IG41A-M7S

Title

Size

Custom

Document Number

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Rev

6.5

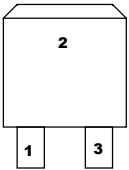
Sheet

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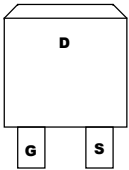
of

34

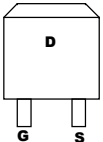
22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



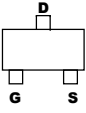
**TO-263**  
B55QS03



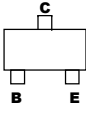
**TO-263**  
2SK3296



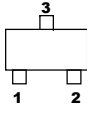
**TO-252**  
20N03  
TM3055TL-S  
45N03  
FDD6030L



**SOT-23**  
2N7002  
SI2303S  
SI2301S



**SOT-23**  
2N3904  
2N3906  
MMBT2907A



**SOT-23**  
BAT54C  
BAT54S



**T0-92**  
LM431  
78L05-D  
LM432



**T0-92**  
2N2222A  
2N2097A



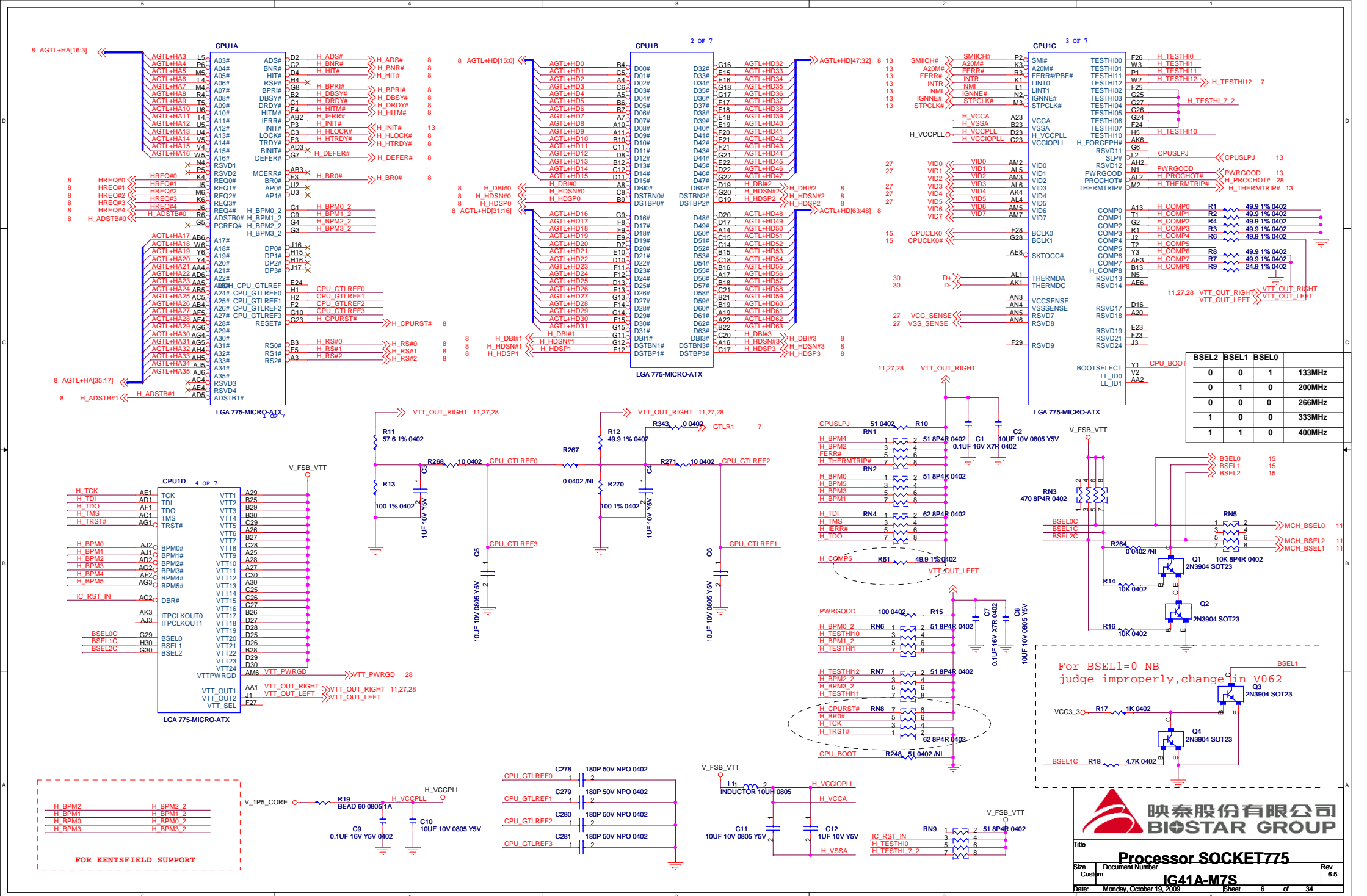
**T0-92**  
HSD882-D

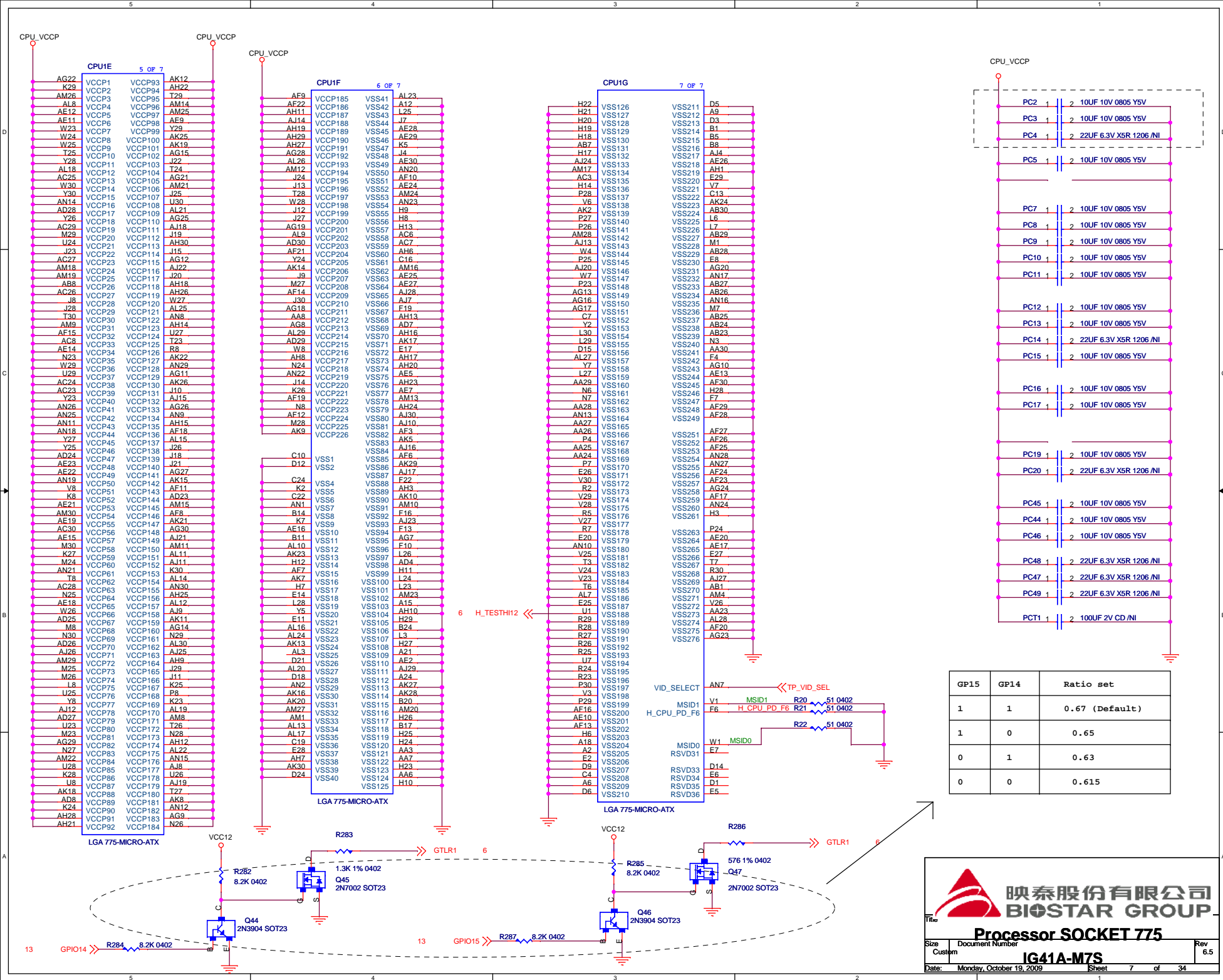


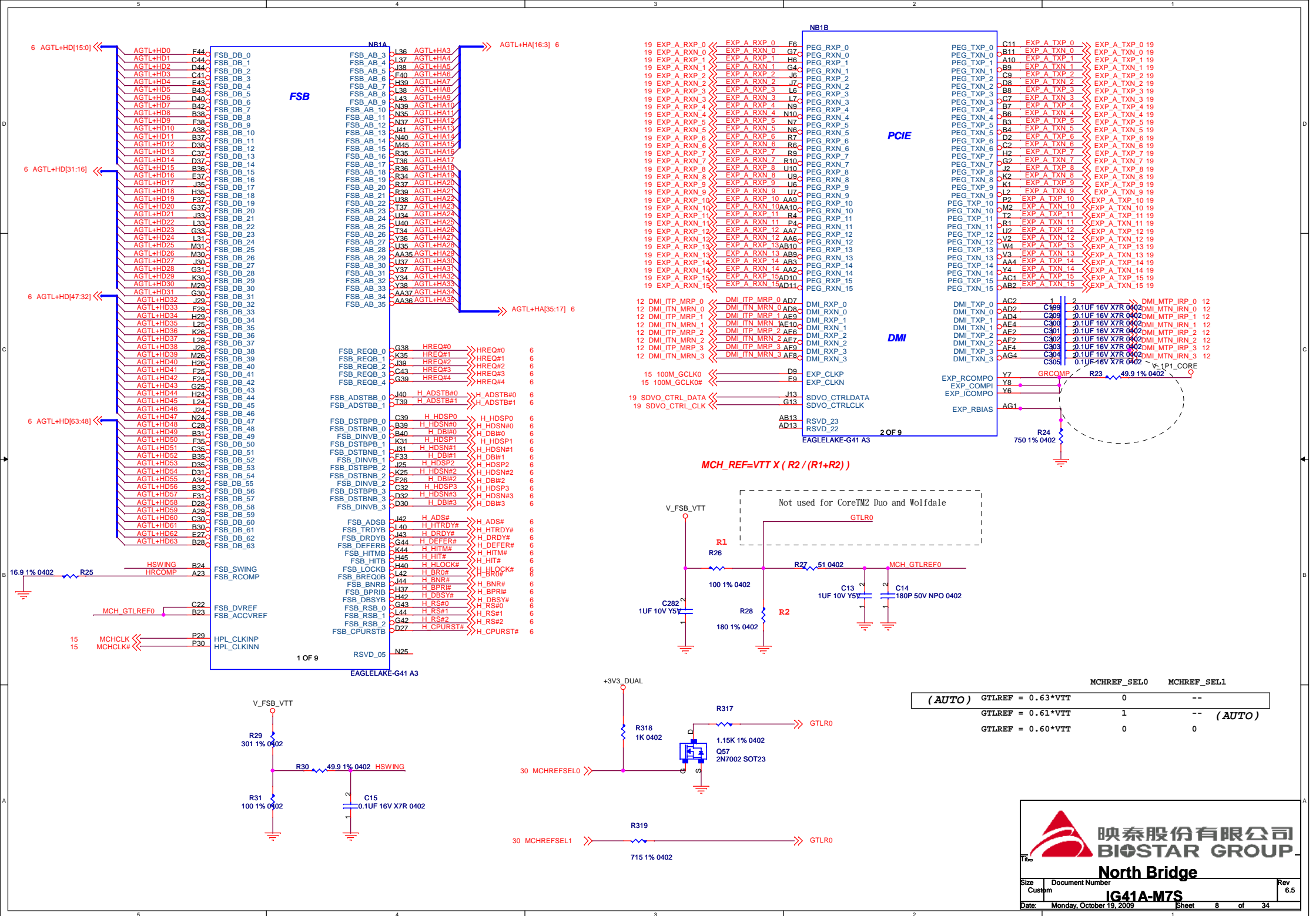
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Component Size

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16,18 DDR\_MAA[0..14] >> DDR\_MAA[0..14]

### NB1C

DDR\_MAA0 BC41  
DDR\_MAA1 BC35  
DDR\_MAA2 BB32  
DDR\_MAA3 BC32  
DDR\_MAA4 BD32  
DDR\_MAA5 BB31  
DDR\_MAA6 AY31  
DDR\_MAA7 BA31  
DDR\_MAA8 BD31  
DDR\_MAA9 BD30  
DDR\_MAA10 AW43  
DDR\_MAA11 BC30  
DDR\_MAA12 BB30  
DDR\_MAA13 AM42  
DDR\_MAA14 BD28

DDR\_A\_MA\_0  
DDR\_A\_MA\_1  
DDR\_A\_MA\_2  
DDR\_A\_MA\_3  
DDR\_A\_MA\_4  
DDR\_A\_MA\_5  
DDR\_A\_MA\_6  
DDR\_A\_MA\_7  
DDR\_A\_MA\_8  
DDR\_A\_MA\_9  
DDR\_A\_MA\_10  
DDR\_A\_MA\_11  
DDR\_A\_MA\_12  
DDR\_A\_MA\_13  
DDR\_A\_MA\_14

DDR\_A\_DQS\_0  
DDR\_A\_DQS\_1  
DDR\_A\_DQS\_2  
DDR\_A\_DQS\_3  
DDR\_A\_DQS\_4  
DDR\_A\_DQS\_5  
DDR\_A\_DQS\_6  
DDR\_A\_DQS\_7

BC5 DDR\_DQS\_P\_0 <<DDR\_DQS\_P\_0 16  
BD4 DDR\_DQS\_N\_0 <<DDR\_DQS\_N\_0 16  
BC3 DDR\_DM0 <<DDR\_DM0 16  
BC2 DDR\_MD0  
BD3 DDR\_MD1  
BD7 DDR\_MD2  
BD7 DDR\_MD3  
BD2 DDR\_MD4  
BA3 DDR\_MD5  
BE6 DDR\_MD6  
BD6 DDR\_MD7

DDR\_A\_DQS\_1  
DDR\_A\_DQS\_1  
DDR\_A\_DQS\_1

BB8 DDR\_DM8  
AY8 DDR\_DM9  
BD11 DDR\_DM10  
BC7 DDR\_DM11  
BE8 DDR\_DM12  
BD10 DDR\_DM13  
AY11 DDR\_DM15

DDR\_A\_DQ\_8  
DDR\_A\_DQ\_9  
DDR\_A\_DQ\_10  
DDR\_A\_DQ\_11  
DDR\_A\_DQ\_12  
DDR\_A\_DQ\_13  
DDR\_A\_DQ\_14  
DDR\_A\_DQ\_15

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQS\_2  
DDR\_A\_DQS\_2  
DDR\_A\_DQS\_2

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQ\_16  
DDR\_A\_DQ\_17  
DDR\_A\_DQ\_18  
DDR\_A\_DQ\_19  
DDR\_A\_DQ\_20  
DDR\_A\_DQ\_21  
DDR\_A\_DQ\_22  
DDR\_A\_DQ\_23

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQS\_3  
DDR\_A\_DQS\_3  
DDR\_A\_DQS\_3

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQ\_24  
DDR\_A\_DQ\_25  
DDR\_A\_DQ\_26  
DDR\_A\_DQ\_27  
DDR\_A\_DQ\_28  
DDR\_A\_DQ\_29  
DDR\_A\_DQ\_30  
DDR\_A\_DQ\_31

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQS\_4  
DDR\_A\_DQS\_4  
DDR\_A\_DQS\_4

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQ\_32  
DDR\_A\_DQ\_33  
DDR\_A\_DQ\_34  
DDR\_A\_DQ\_35  
DDR\_A\_DQ\_36  
DDR\_A\_DQ\_37  
DDR\_A\_DQ\_38  
DDR\_A\_DQ\_39

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQS\_5  
DDR\_A\_DQS\_5  
DDR\_A\_DQS\_5

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQ\_40  
DDR\_A\_DQ\_41  
DDR\_A\_DQ\_42  
DDR\_A\_DQ\_43  
DDR\_A\_DQ\_44  
DDR\_A\_DQ\_45  
DDR\_A\_DQ\_46  
DDR\_A\_DQ\_47

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQS\_6  
DDR\_A\_DQS\_6  
DDR\_A\_DQS\_6

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQ\_48  
DDR\_A\_DQ\_49  
DDR\_A\_DQ\_50  
DDR\_A\_DQ\_51  
DDR\_A\_DQ\_52  
DDR\_A\_DQ\_53  
DDR\_A\_DQ\_54  
DDR\_A\_DQ\_55

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQS\_7  
DDR\_A\_DQS\_7  
DDR\_A\_DQS\_7

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A\_DQ\_56  
DDR\_A\_DQ\_57  
DDR\_A\_DQ\_58  
DDR\_A\_DQ\_59  
DDR\_A\_DQ\_60  
DDR\_A\_DQ\_61  
DDR\_A\_DQ\_62  
DDR\_A\_DQ\_63

BD15 DDR\_DQS\_P\_2 <<DDR\_DQS\_P\_2 16  
BB15 DDR\_DQS\_N\_2 <<DDR\_DQS\_N\_2 16  
BD14 DDR\_DM2 <<DDR\_DM2 16  
BB14 DDR\_DM16  
BC14 DDR\_DM17  
BC16 DDR\_DM18  
BB16 DDR\_DM19  
BC11 DDR\_DM20  
BE12 DDR\_DM21  
BA15 DDR\_DM22  
BD16 DDR\_DM23

DDR\_A

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EAGLELAKE-G41 A3

17,18 DDRB\_MBA[0..14] >> DDRB\_MBA[0..14]

### NB1D

DDR\_B\_MBA0 BD24  
DDR\_B\_MBA1 BB24  
DDR\_B\_MBA2 BB24  
DDR\_B\_MBA3 BB23  
DDR\_B\_MBA4 BB22  
DDR\_B\_MBA5 BB22  
DDR\_B\_MBA6 BB22  
DDR\_B\_MBA7 BB20  
DDR\_B\_MBA8 BB20  
DDR\_B\_MBA9 BB20  
DDR\_B\_MBA10 BC26  
DDR\_B\_MBA11 BD19  
DDR\_B\_MBA12 BB19  
DDR\_B\_MBA13 BB19  
DDR\_B\_MBA14 BA19

DDR\_B\_MA\_0  
DDR\_B\_MA\_1  
DDR\_B\_MA\_2  
DDR\_B\_MA\_3  
DDR\_B\_MA\_4  
DDR\_B\_MA\_5  
DDR\_B\_MA\_6  
DDR\_B\_MA\_7  
DDR\_B\_MA\_8  
DDR\_B\_MA\_9  
DDR\_B\_MA\_10  
DDR\_B\_MA\_11  
DDR\_B\_MA\_12  
DDR\_B\_MA\_13  
DDR\_B\_MA\_14

17,18 DDRB\_WE# <<DDRB\_WE# 16  
17,18 DDRB\_CAS# <<DDRB\_CAS# 16  
17,18 DDRB\_RAS# <<DDRB\_RAS# 16

17,18 DDRB\_BA0 <<DDR\_BA0 16  
17,18 DDRB\_BA1 <<DDR\_BA1 16  
17,18 DDRB\_BA2 <<DDR\_BA2 16

17,18 DDRB\_CS#0 <<DDRB\_CS#0 16  
17,18 DDRB\_CS#1 <<DDRB\_CS#1 16

17,18 DDRB\_CKE0 <<DDR\_B\_CKE0 16  
17,18 DDRB\_CKE1 <<DDR\_B\_CKE1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

17,18 SODT\_0 <<SODT\_0 16  
17,18 SODT\_1 <<SODT\_1 16

DDR\_B

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DDR\_B\_DQS\_0  
DDR\_B\_DQS\_1  
DDR\_B\_DQS\_2

AW8 DDRB\_DQS\_P\_0 <<DDR\_B\_DQS\_P\_0 17  
AW9 DDRB\_DQS\_N\_0 <<DDR\_B\_DQS\_N\_0 17  
AY6 DDRB\_DM0 <<DDR\_B\_DM0 17

DDR\_B\_DQ\_0  
DDR\_B\_DQ\_1  
DDR\_B\_DQ\_2  
DDR\_B\_DQ\_3  
DDR\_B\_DQ\_4  
DDR\_B\_DQ\_5  
DDR\_B\_DQ\_6  
DDR\_B\_DQ\_7

AV7 DDRB\_MD0  
AW4 DDRB\_MD1  
BA9 DDRB\_MD2  
AU7 DDRB\_MD3  
AU7 DDRB\_MD4  
AU8 DDRB\_MD5  
AW7 DDRB\_MD6  
AY9 DDRB\_MD7

DDR\_B\_DQS\_1  
DDR\_B\_DQS\_1  
DDR\_B\_DQS\_1

AT15 DDRB\_DQS\_P\_1 <<DDR\_B\_DQS\_P\_1 17  
AU15 DDRB\_DQS\_N\_1 <<DDR\_B\_DQS\_N\_1 17  
AR15 DDRB\_DM1 <<DDR\_B\_DM1 17

DDR\_B\_DQ\_8  
DDR\_B\_DQ\_9  
DDR\_B\_DQ\_10  
DDR\_B\_DQ\_11  
DDR\_B\_DQ\_12  
DDR\_B\_DQ\_13  
DDR\_B\_DQ\_14  
DDR\_B\_DQ\_15

AY13 DDRB\_MD8  
AP15 DDRB\_MD9  
AW15 DDRB\_MD10  
AT16 DDRB\_MD11  
AU13 DDRB\_MD12  
AV13 DDRB\_MD13  
AP16 DDRB\_MD14  
AU16 DDRB\_MD15

DDR\_B\_DQS\_2  
DDR\_B\_DQS\_2  
DDR\_B\_DQS\_2

AR20 DDRB\_DQS\_P\_2 <<DDR\_B\_DQS\_P\_2 17  
AU17 DDRB\_DQS\_N\_2 <<DDR\_B\_DQS\_N\_2 17  
AU17 DDRB\_DM2 <<DDR\_B\_DM2 17

DDR\_B\_DQ\_16  
DDR\_B\_DQ\_17  
DDR\_B\_DQ\_18  
DDR\_B\_DQ\_19  
DDR\_B\_DQ\_20  
DDR\_B\_DQ\_21  
DDR\_B\_DQ\_22  
DDR\_B\_DQ\_23

AY17 DDRB\_MD16  
AV17 DDRB\_MD17  
AR21 DDRB\_MD18  
AV20 DDRB\_MD19  
AP17 DDRB\_MD20  
AW16 DDRB\_MD21  
AT20 DDRB\_MD22  
AN20 DDRB\_MD23

DDR\_B\_DQS\_3  
DDR\_B\_DQS\_3  
DDR\_B\_DQS\_3

AU26 DDRB\_DQS\_P\_3 <<DDR\_B\_DQS\_P\_3 17  
AT26 DDRB\_DQS\_N\_3 <<DDR\_B\_DQS\_N\_3 17  
AV25 DDRB\_DM3 <<DDR\_B\_DM3 17

DDR\_B\_DQ\_24  
DDR\_B\_DQ\_25  
DDR\_B\_DQ\_26  
DDR\_B\_DQ\_27  
DDR\_B\_DQ\_28  
DDR\_B\_DQ\_29  
DDR\_B\_DQ\_30  
DDR\_B\_DQ\_31

AT25 DDRB\_MD24  
AV26 DDRB\_MD25  
AU25 DDRB\_MD26  
AV25 DDRB\_MD27  
AV22 DDRB\_MD28  
AR25 DDRB\_MD29  
AP26 DDRB\_MD30  
AR29 DDRB\_MD31

DDR\_B\_DQS\_4  
DDR\_B\_DQS\_4  
DDR\_B\_DQS\_4

AR38 DDRB\_DQS\_P\_4 <<DDR\_B\_DQS\_P\_4 17  
AR37 DDRB\_DQS\_N\_4 <<DDR\_B\_DQS\_N\_4 17  
AU39 DDRB\_DM4 <<DDR\_B\_DM4 17

DDR\_B\_DQ\_32  
DDR\_B\_DQ\_33  
DDR\_B\_DQ\_34  
DDR\_B\_DQ\_35  
DDR\_B\_DQ\_36  
DDR\_B\_DQ\_37  
DDR\_B\_DQ\_38  
DDR\_B\_DQ\_39

AR36 DDRB\_MD32  
AU38 DDRB\_MD33  
AN35 DDRB\_MD34  
AN37 DDRB\_MD35  
AV39 DDRB\_MD36  
AW39 DDRB\_MD37  
AU40 DDRB\_MD38  
AU41 DDRB\_MD39

DDR\_B\_DQS\_5  
DDR\_B\_DQS\_5  
DDR\_B\_DQS\_5

AK34 DDRB\_DQS\_P\_5 <<DDR\_B\_DQS\_P\_5 17  
AL34 DDRB\_DQS\_N\_5 <<DDR\_B\_DQS\_N\_5 17  
AL37 DDRB\_DM5 <<DDR\_B\_DM5 17

DDR\_B\_DQ\_40  
DDR\_B\_DQ\_41  
DDR\_B\_DQ\_42  
DDR\_B\_DQ\_43  
DDR\_B\_DQ\_44  
DDR\_B\_DQ\_45  
DDR\_B\_DQ\_46  
DDR\_B\_DQ\_47

AL35 DDRB\_MD40  
AL36 DDRB\_MD41  
AK36 DDRB\_MD42  
AJ34 DDRB\_MD43  
AN39 DDRB\_MD44  
AN40 DDRB\_MD45  
AK37 DDRB\_MD46  
AL39 DDRB\_MD47

DDR\_B\_DQS\_6  
DDR\_B\_DQS\_6  
DDR\_B\_DQS\_6

AF37 DDRB\_DQS\_P\_6 <<DDR\_B\_DQS\_P\_6 17  
AF36 DDRB\_DQS\_N\_6 <<DDR\_B\_DQS\_N\_6 17  
AJ35 DDRB\_DM6 <<DDR\_B\_DM6 17

DDR\_B\_DQ\_48  
DDR\_B\_DQ\_49  
DDR\_B\_DQ\_50  
DDR\_B\_DQ\_51  
DDR\_B\_DQ\_52  
DDR\_B\_DQ\_53  
DDR\_B\_DQ\_54  
DDR\_B\_DQ\_55

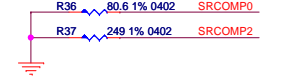
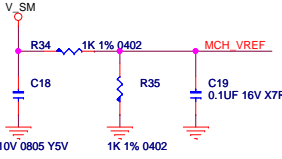
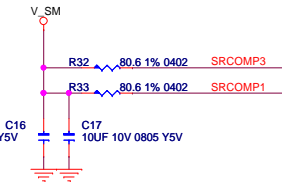
AJ38 DDRB\_MD48  
AJ37 DDRB\_MD49  
AF38 DDRB\_MD50  
AE37 DDRB\_MD51  
AK40 DDRB\_MD52  
AJ40 DDRB\_MD53  
AE34 DDRB\_MD54  
AE35 DDRB\_MD55

DDR\_B\_DQS\_7  
DDR\_B\_DQS\_7  
DDR\_B\_DQS\_7

AB35 DDRB\_DQS\_P\_7 <<DDR\_B\_DQS\_P\_7 17  
AD35 DDRB\_DQS\_N\_7 <<DDR\_B\_DQS\_N\_7 17  
AD37 DDRB\_DM7 <<DDR\_B\_DM7 17

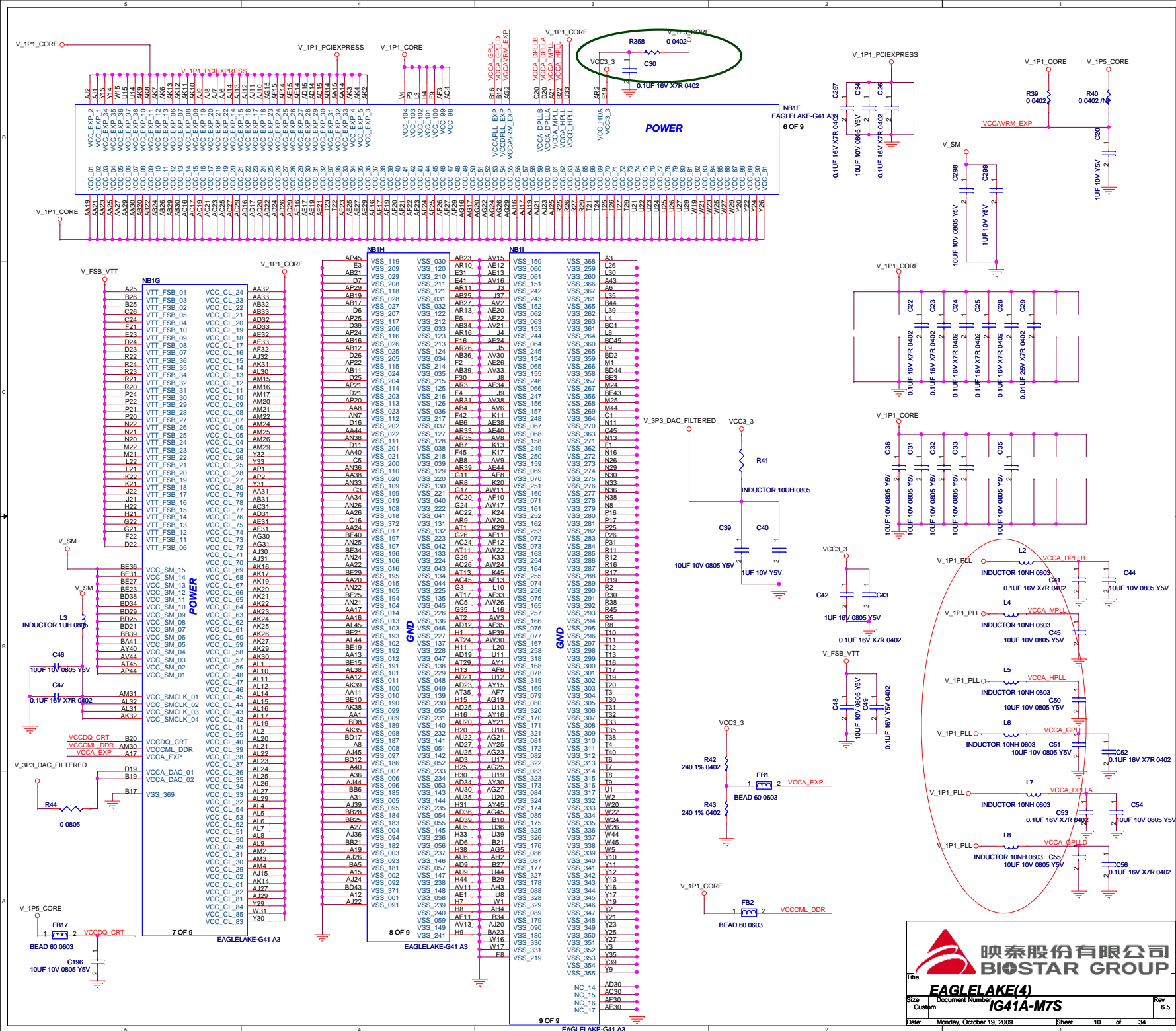
DDR\_B\_DQ\_56  
DDR\_B\_DQ\_57  
DDR\_B\_DQ\_58  
DDR\_B\_DQ\_59  
DDR\_B\_DQ\_60  
DDR\_B\_DQ\_61  
DDR\_B\_DQ\_62  
DDR\_B\_DQ\_63

AD40 DDRB\_MD56  
AD38 DDRB\_MD57  
AB40 DDRB\_MD58  
AA39 DDRB\_MD59  
AE36 DDRB\_MD60  
AE39 DDRB\_MD61  
AB37 DDRB\_MD62  
AB38 DDRB\_MD63

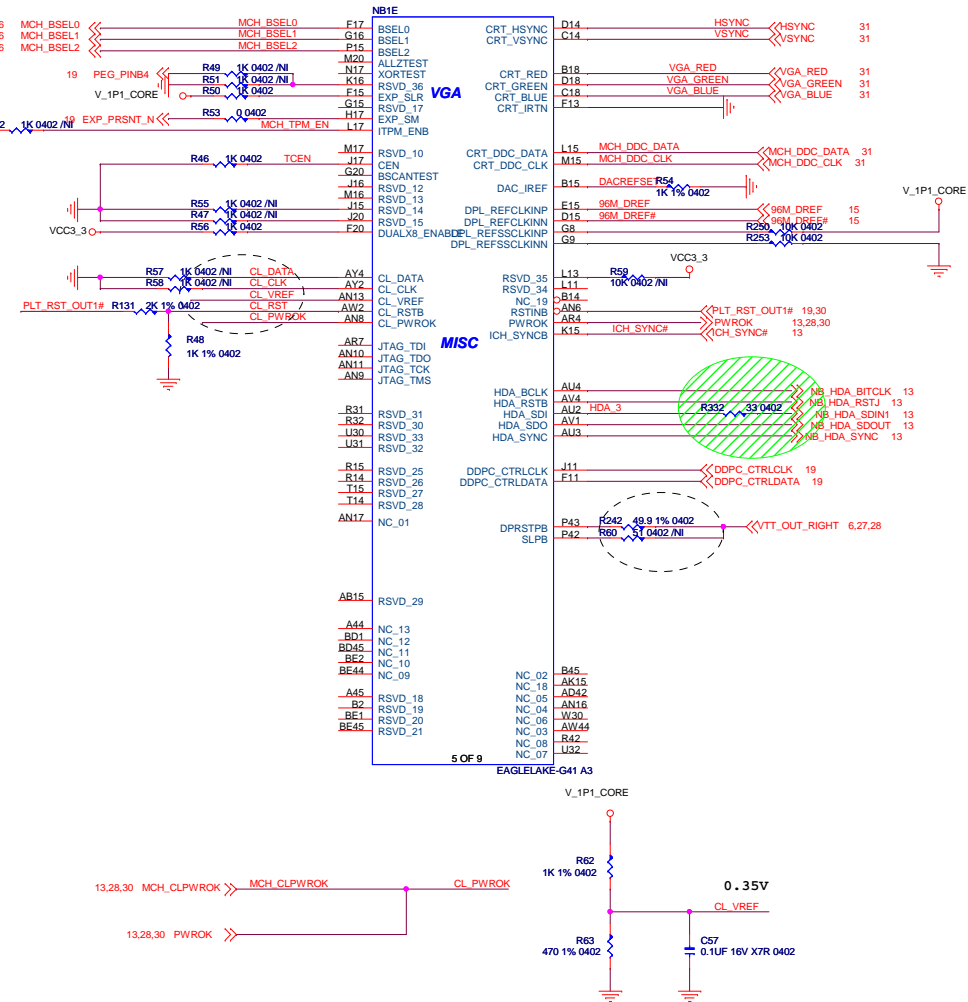


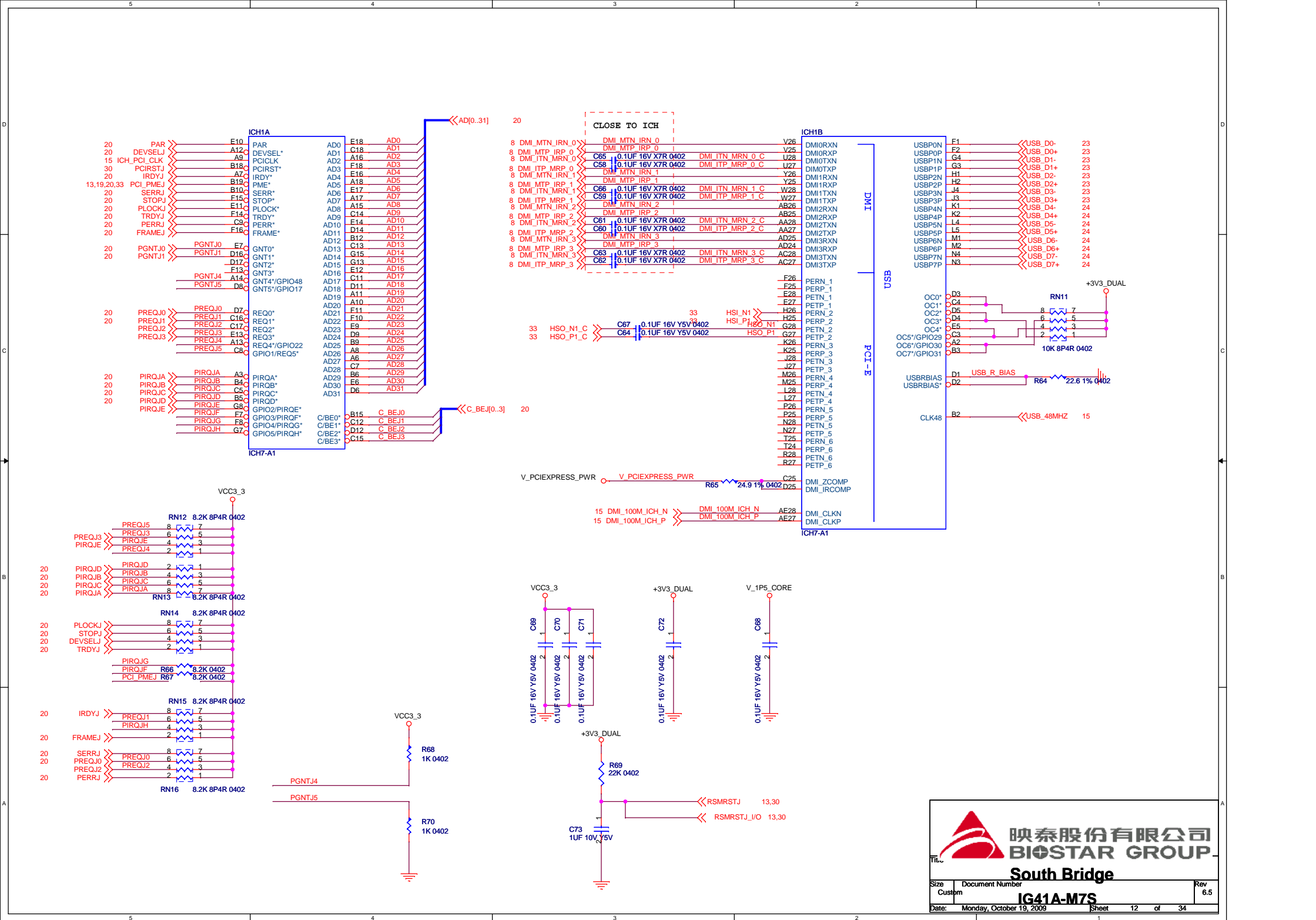
16 DDR\_MD[0..63] >>  
17 DDR\_MD[0..63] >>

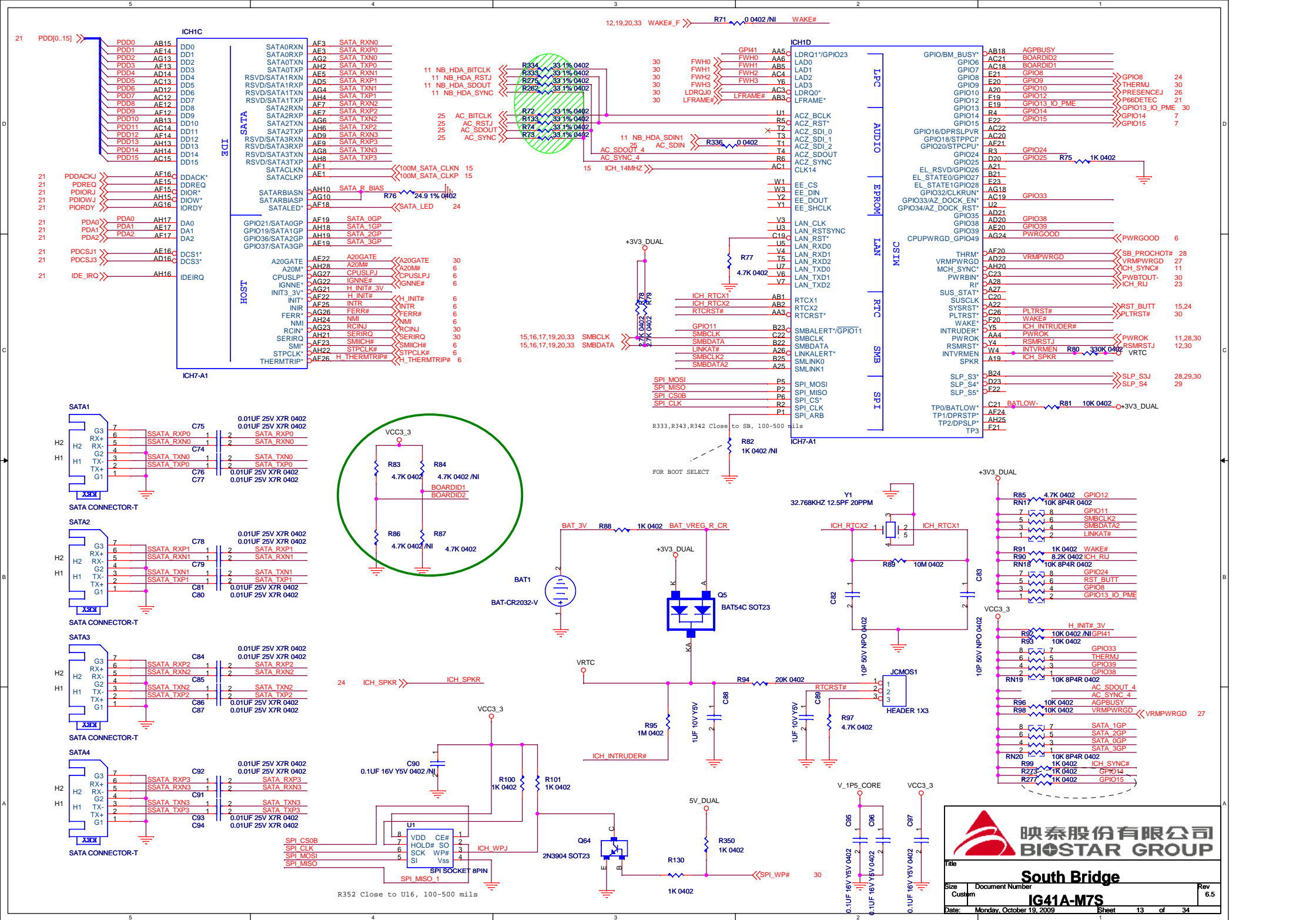
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BIOSAR GROUP  
North Bridge  
IG41A-M7S  
Rev 6.5  
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MCH Enable Strap  
Pulldown:Enable TPM(Default)  
Float:Disable TPM

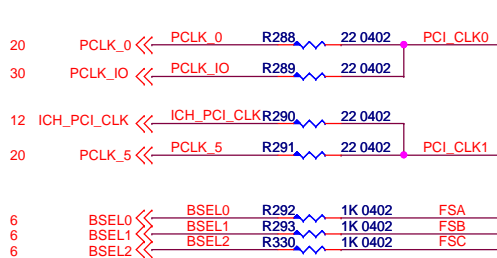
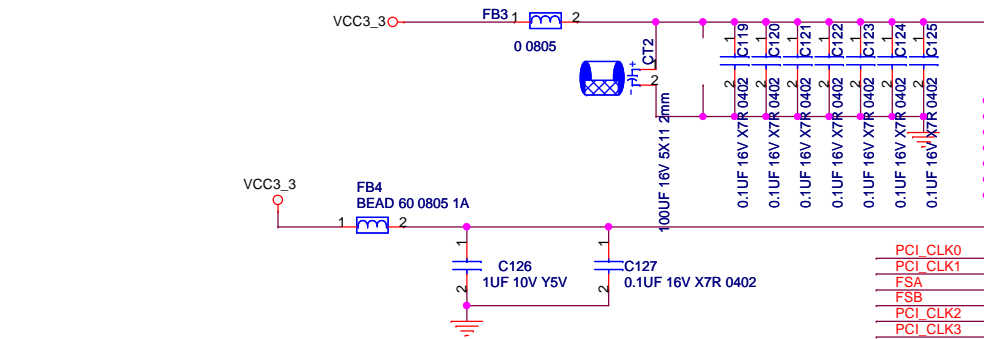




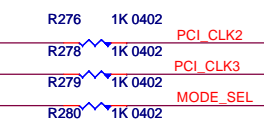
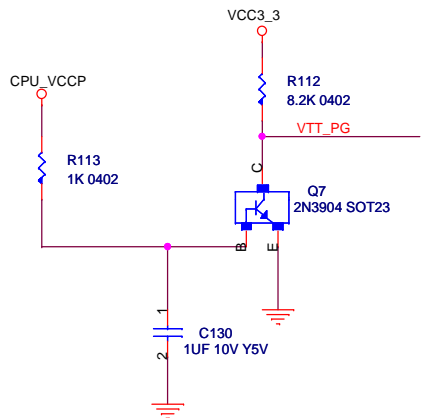








BSEL2	BSEL1	BSEL0	
0	0	1	133MHz
0	1	0	200MHz
0	0	0	266MHz
1	0	0	333MHz



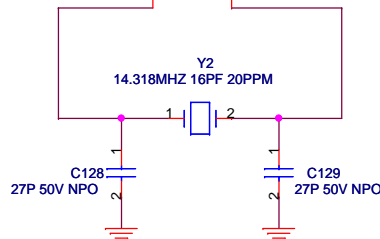
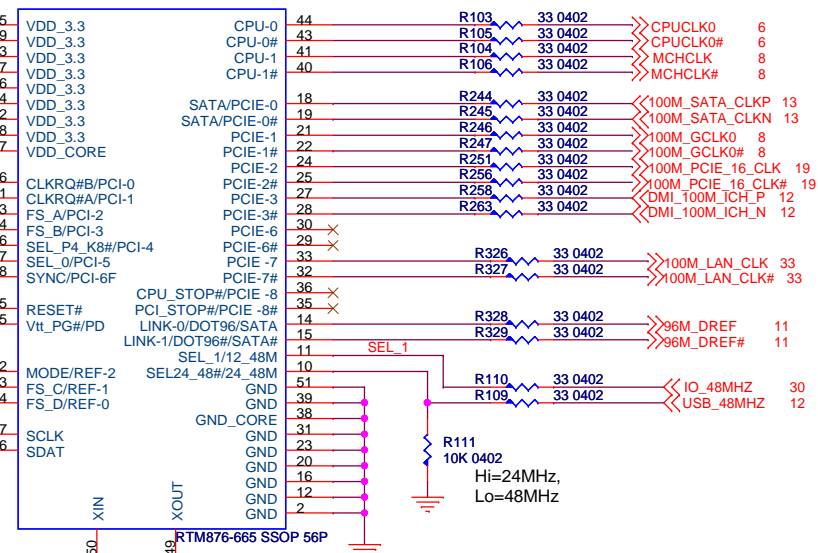
Pin6 PCIF\_CLK1=SEL P4/K8(internal pull high)  
Hi = P4 0.8V push-pull CPU clock  
Lo = K8 3.3V push-pull CPU clock

Pin52 MOD\_SEL=SEL PIN35/36=PCIE-8(internal pull low)  
MODE=0 PIN35/36 is PCIE8#/PCIE8  
MODE=1 PIN35/36 is PCI\_STOP#/CPU\_STOP#

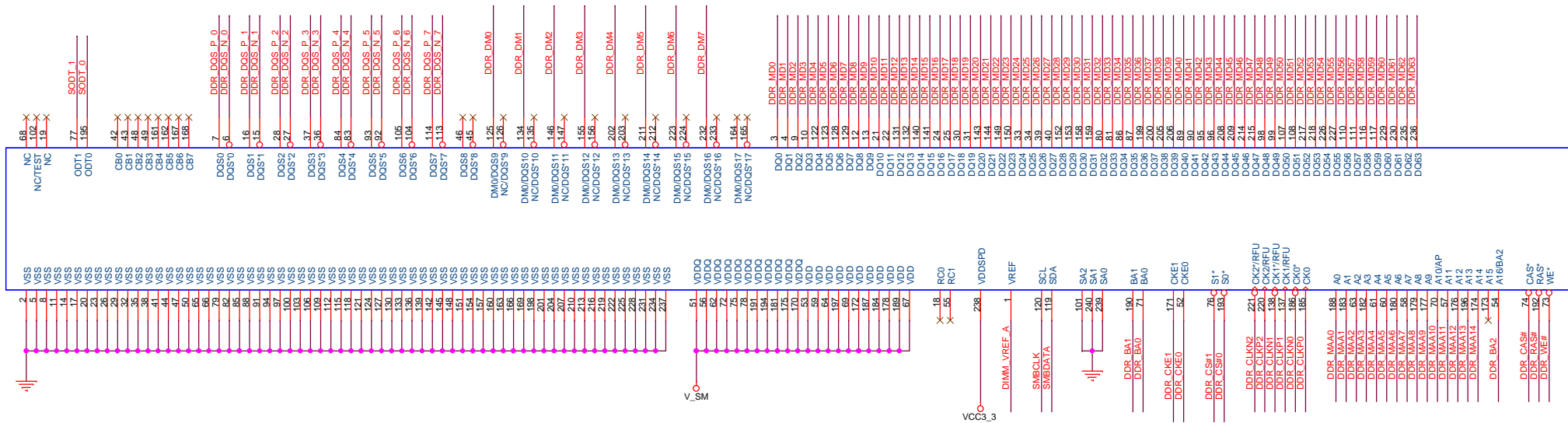
Pin11 Sel-1	Pin7 Sel-0	Pin7/8 Link/DOT/SATA	Pin11/12 SATA/PCIE	12-48M	Chipset
0	0	Link	SATA	12M	Sis
0	1	DOT	SATA	48M	Intel W/GFX
1	0	Link	PCIE	48M	VIA
1	1	SATA	PCIE	48M	Intel

For Intel Chipset w/o GFX (SEL-1/0 = 11)  
DOT96 is not necessary

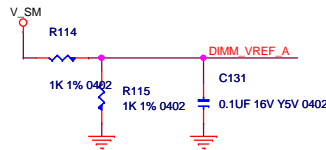
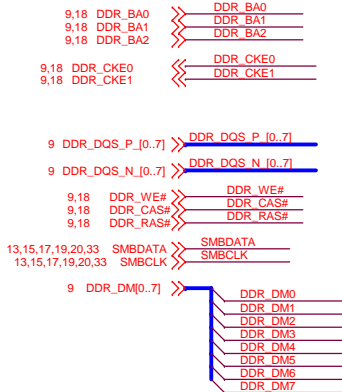
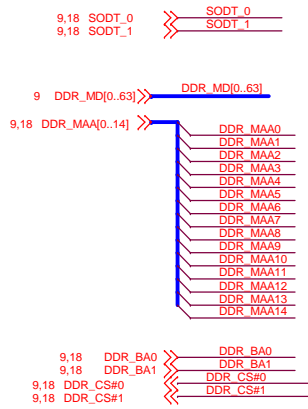
## RTM876-665




Title			
CLK GEN / BIOS (FWH)			
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DDR2\_A1  
DDR2-240 pin-T





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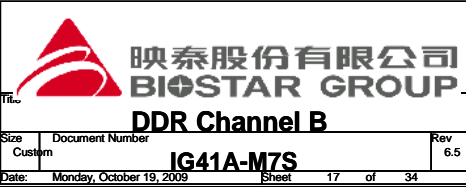
BIOSAR GROUP

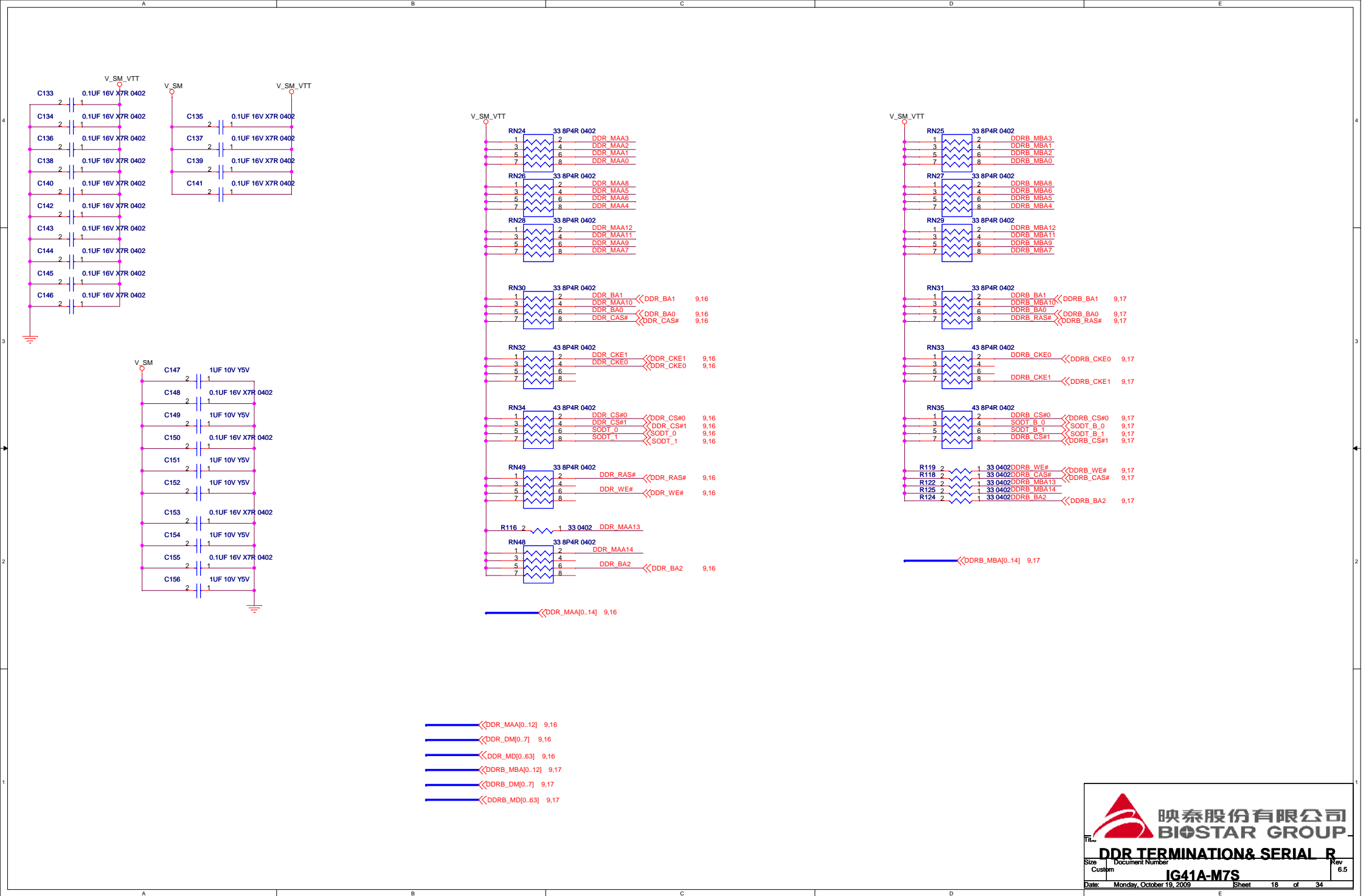
DDR Channel A

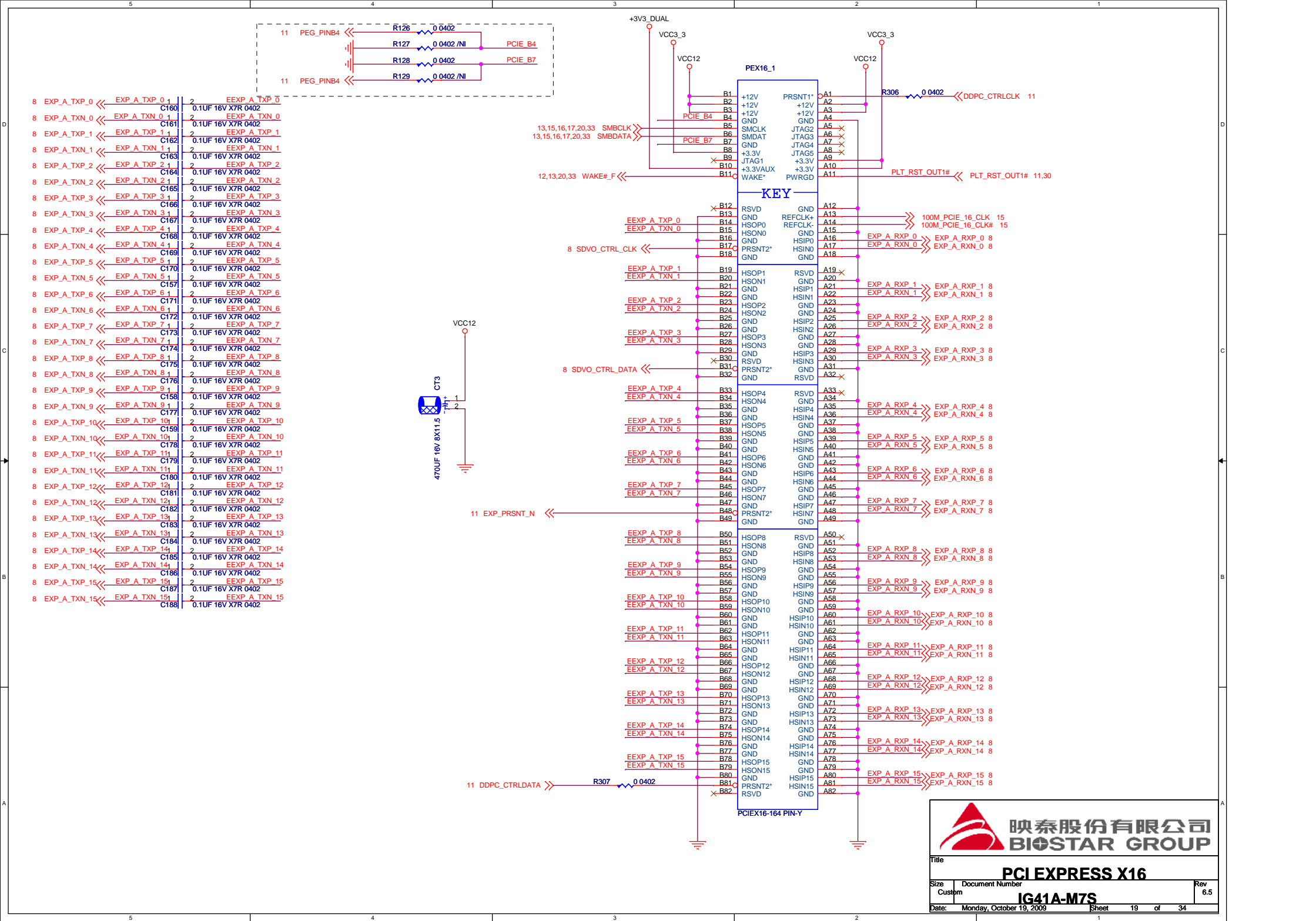
IG41A-M7S

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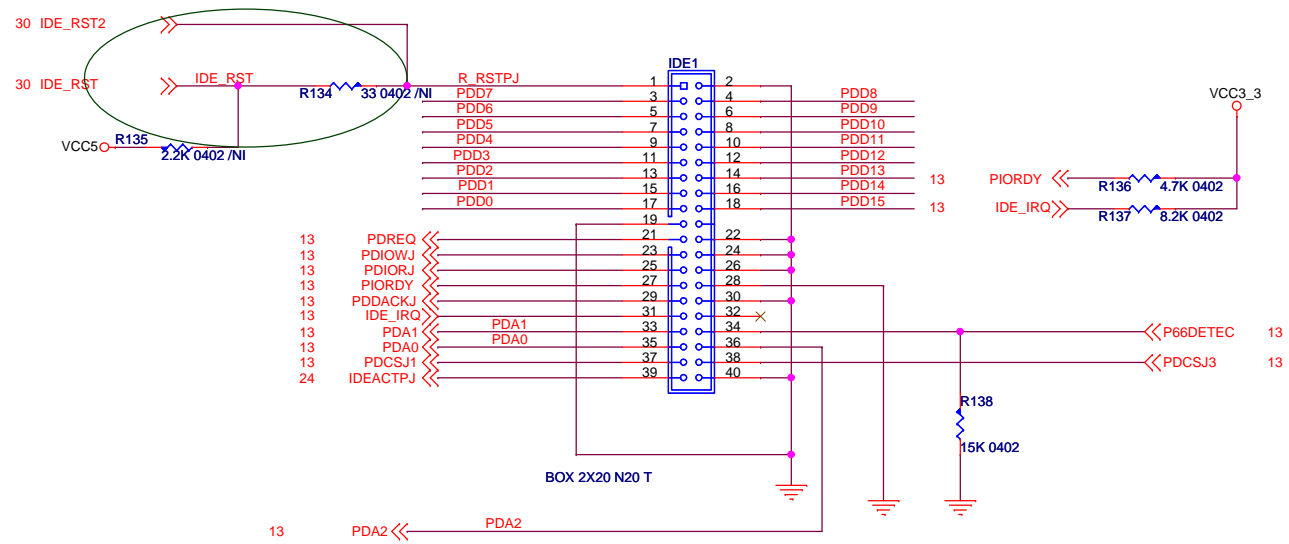




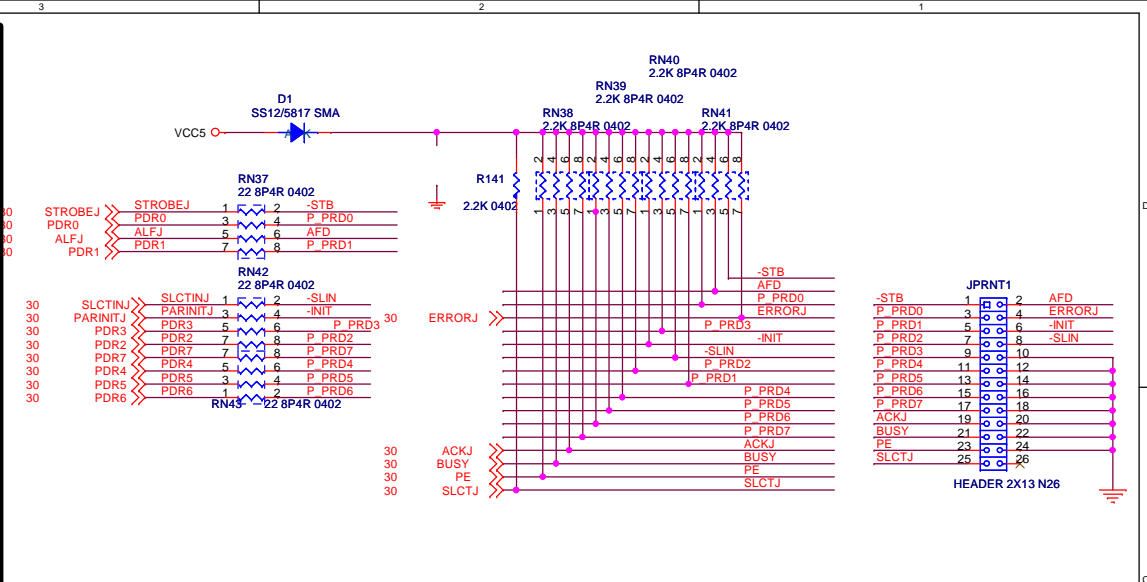
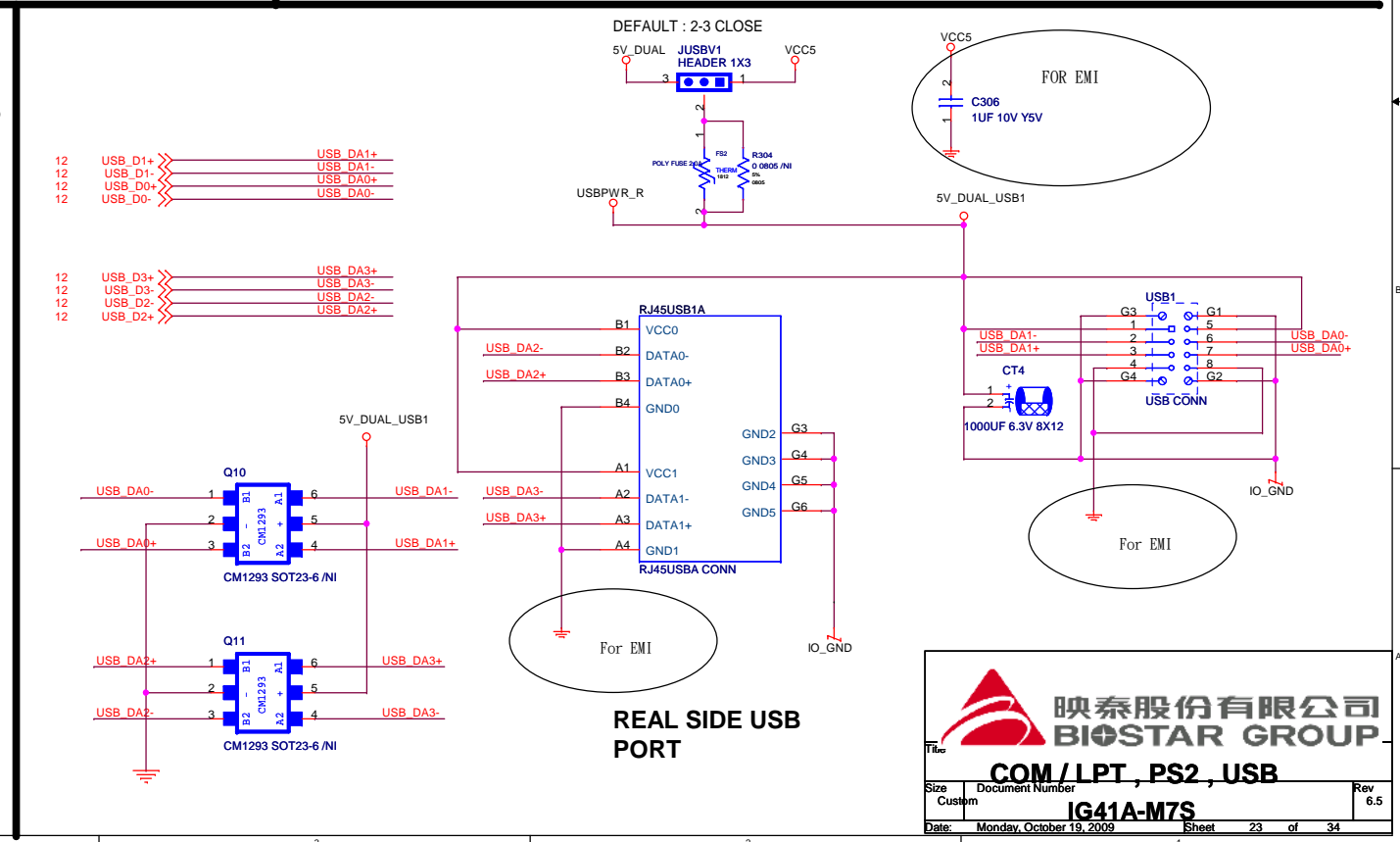




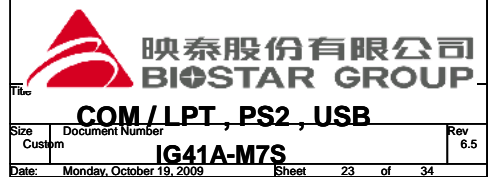


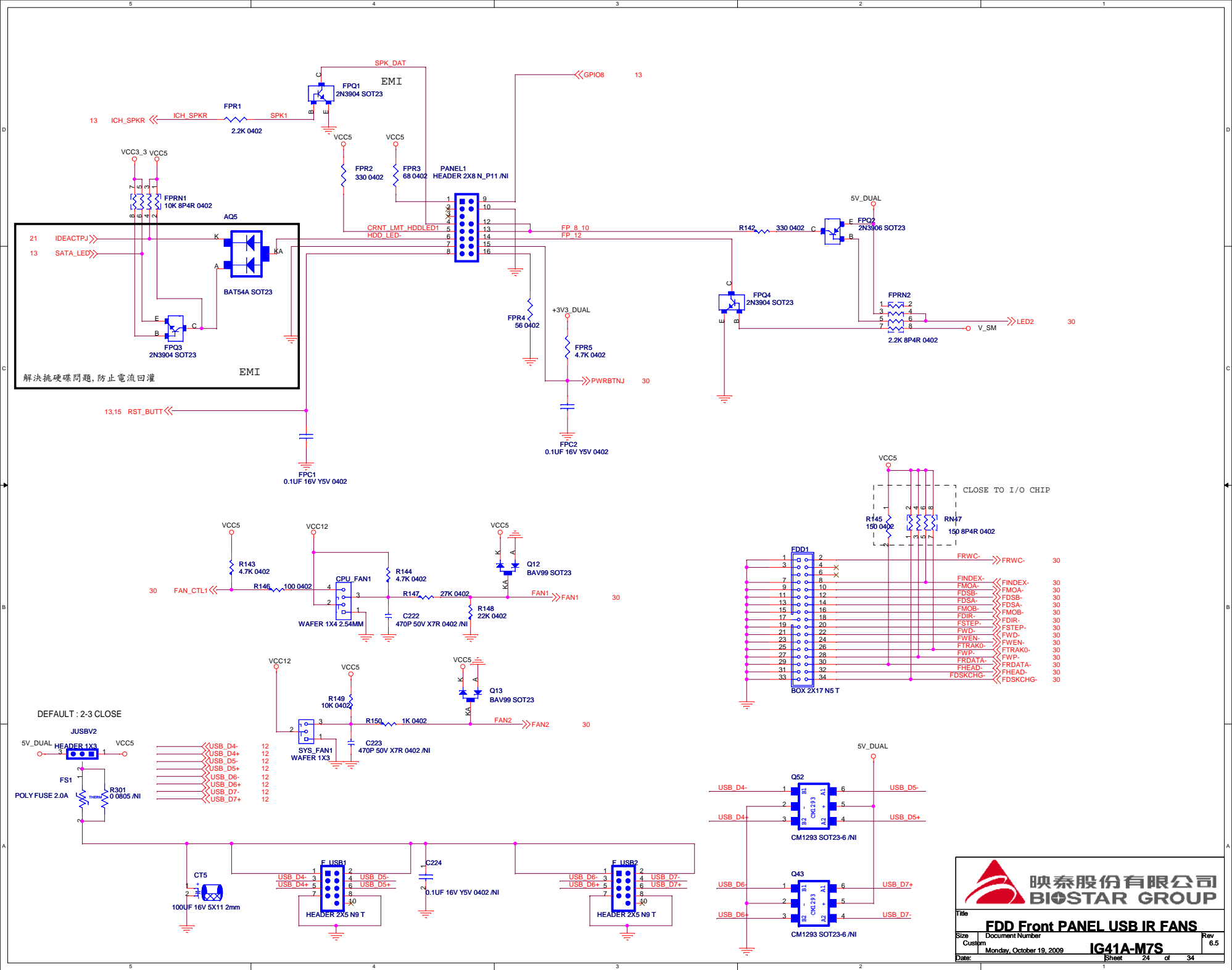




COM  
PORTPS2  
PORT

## REAL SIDE USB PORT



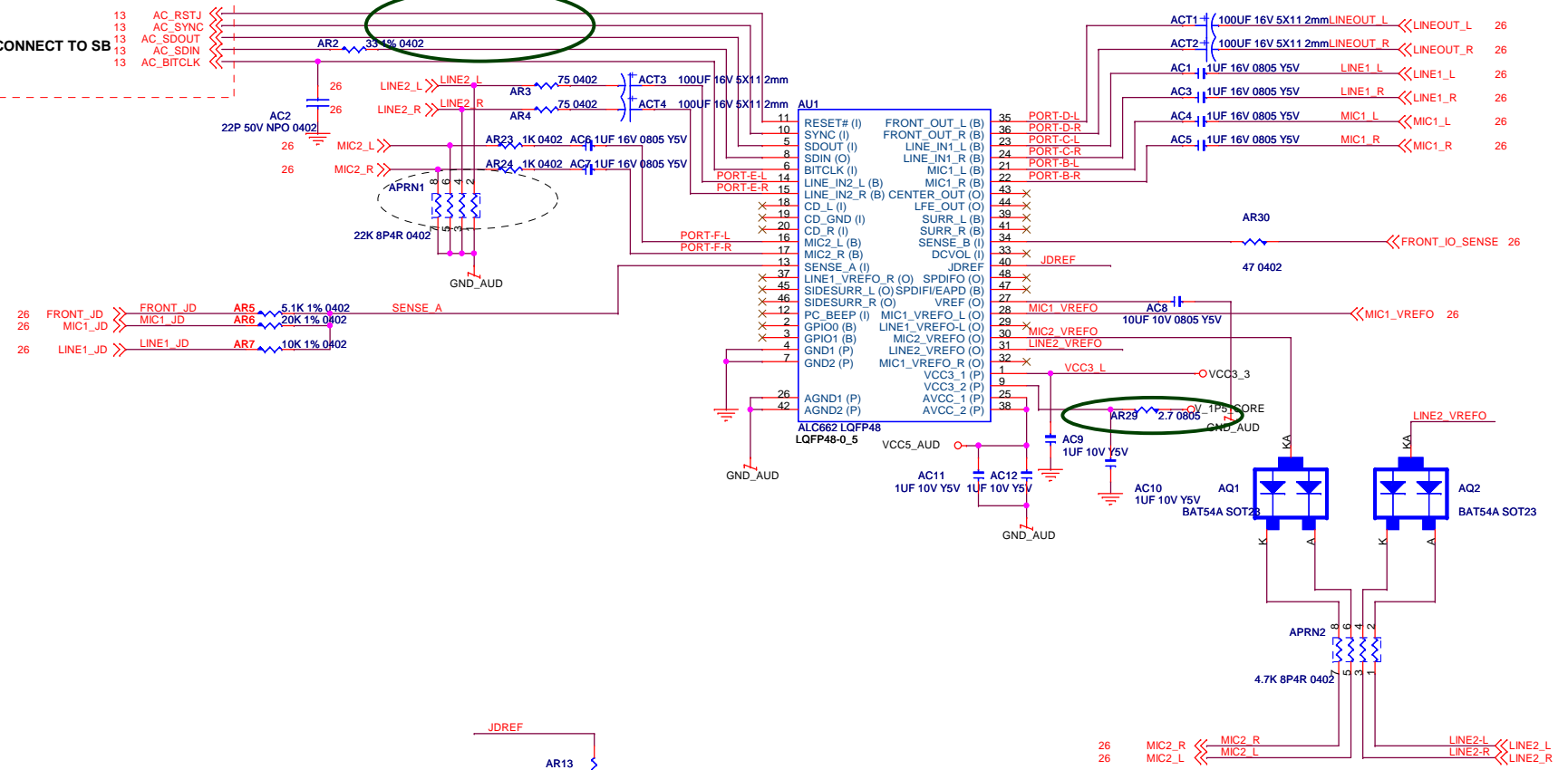




CD\_IN

CONNECT TO SB


- 13 AC\_RSTJ
- 13 AC\_SYNC
- 13 AC\_SDOUT
- 13 AC\_SDIN
- 13 AC\_BITCLK



JDREF  
AR13 20K 1% 0402  
GND\_AUD  
PLACE CLOSE TO CODEC

AR14 0 0805  
R0603  
GND\_AUD

AR15 0 0805 /NI  
R0603  
IO\_GND GND\_AUD



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BIOSTAR GROUP

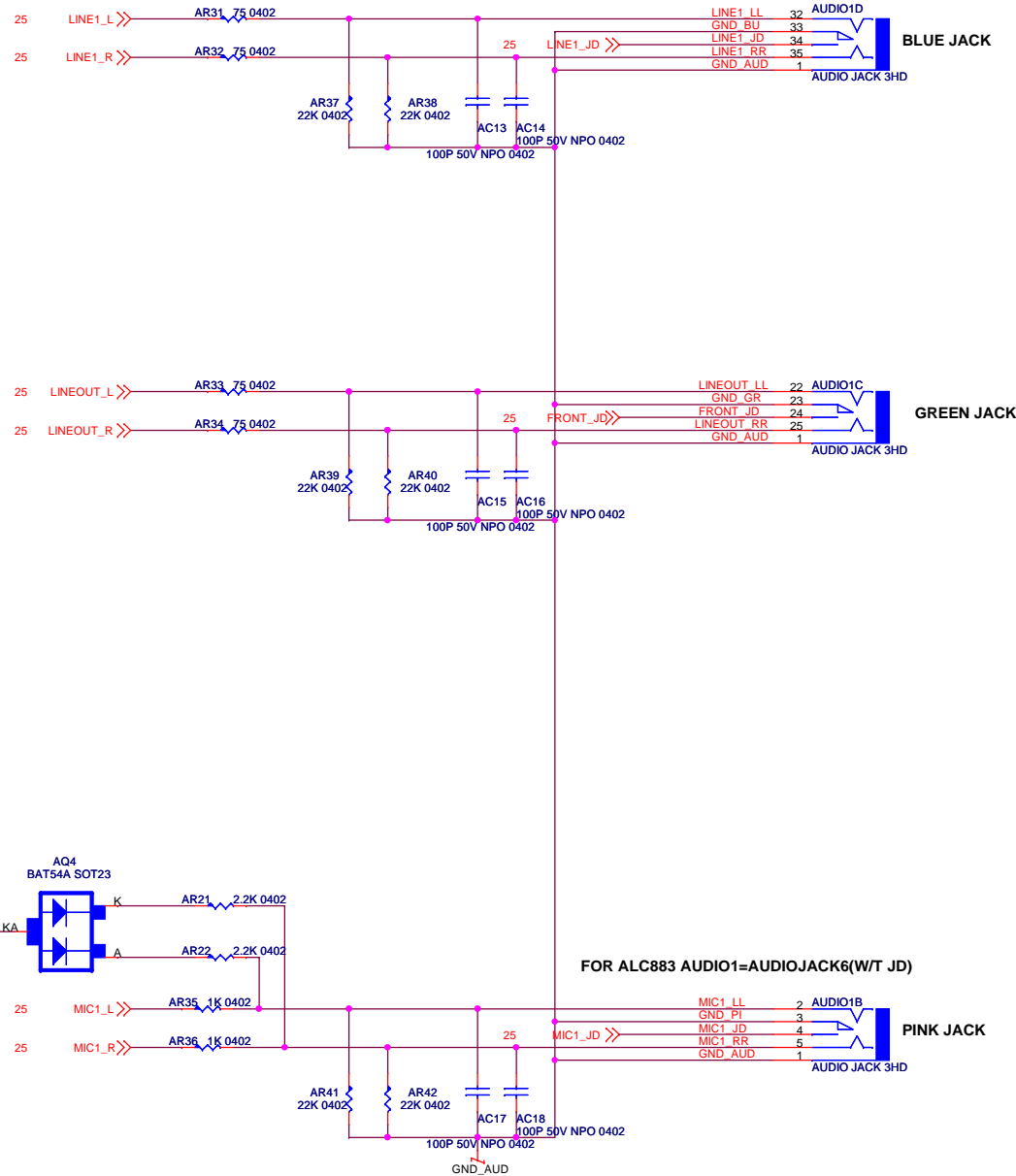
CMI 9880,9761A-3,ALC880

IG41A-M7S

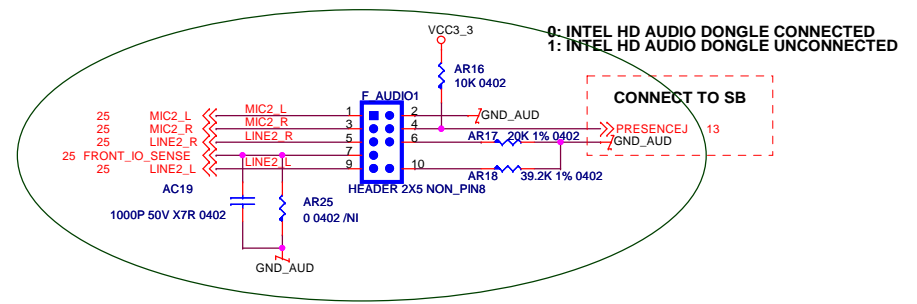
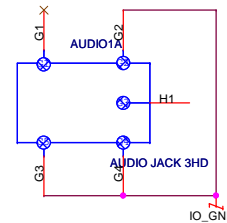
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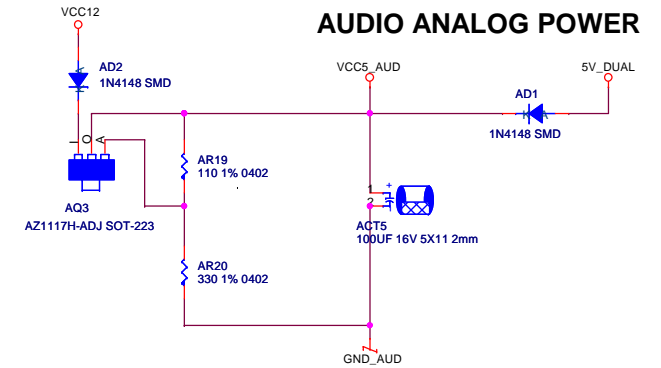
## Rear Panel Onboard Analog I/O



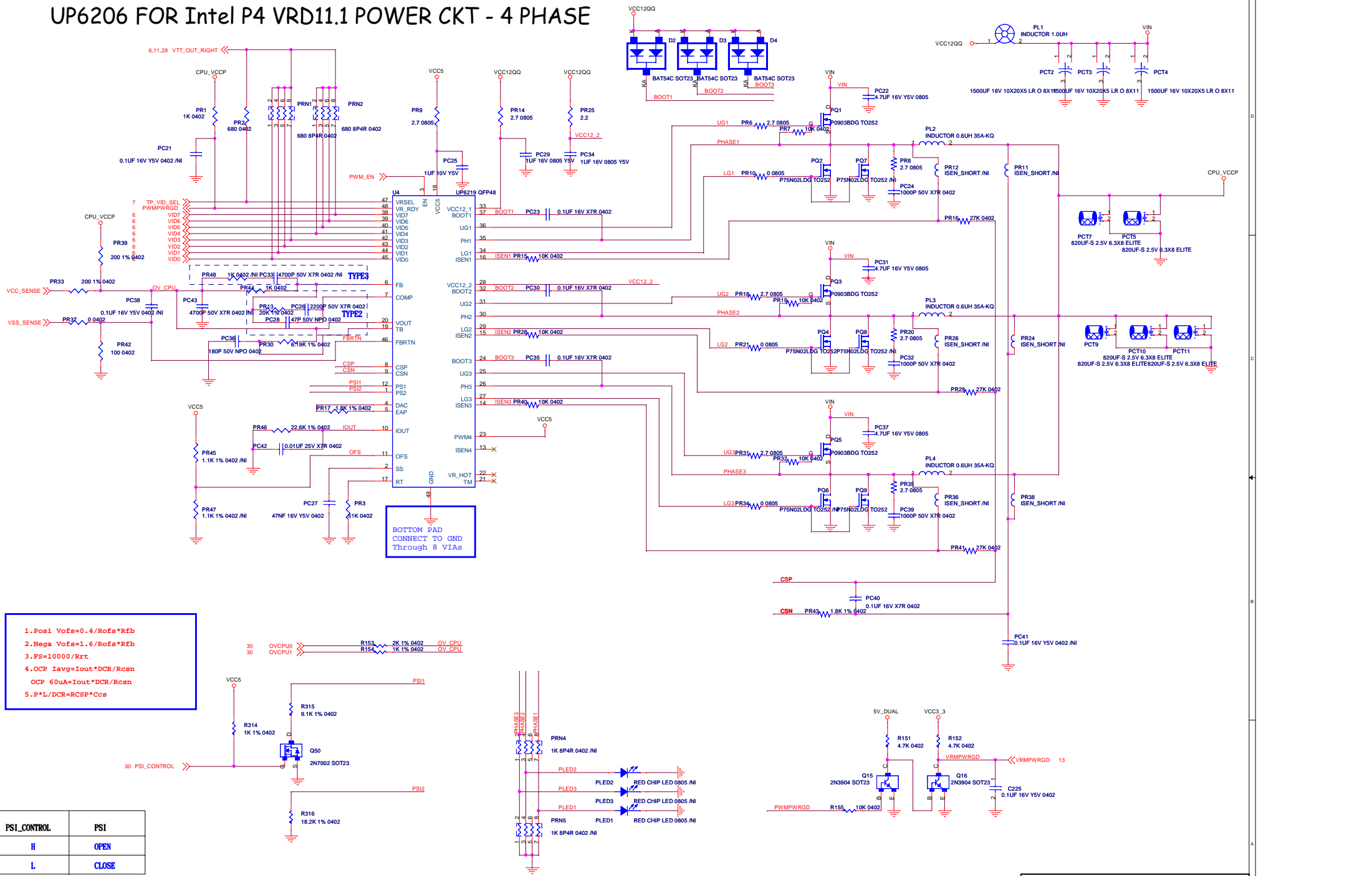
FOR ALC883 AUDIO1=AUDIOJACK6(W/T JD)



## AUDIO ANALOG POWER

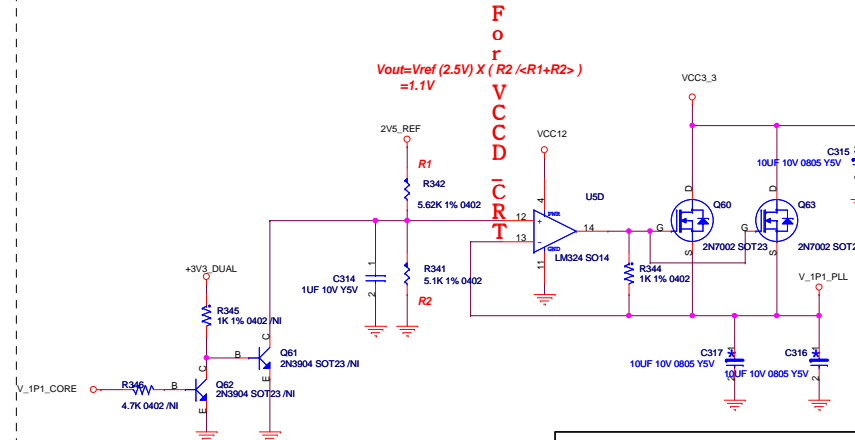
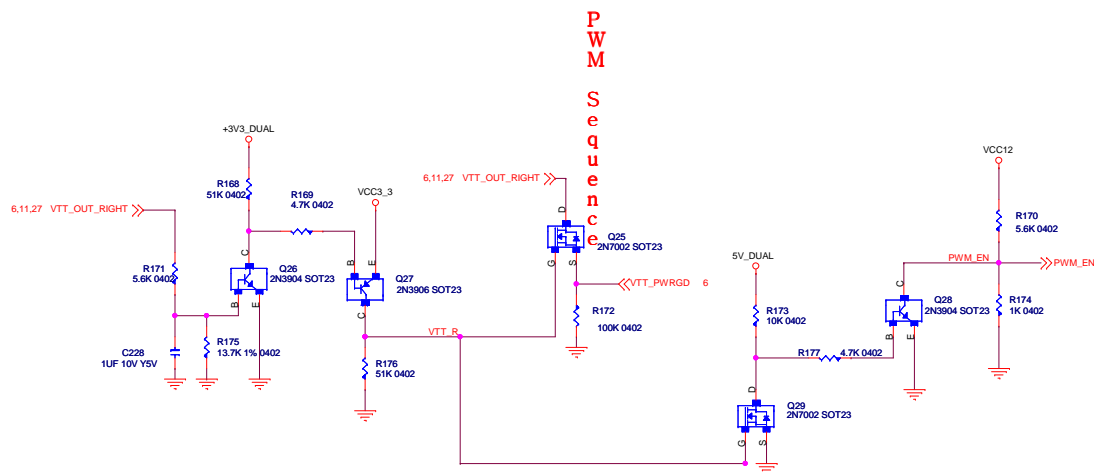
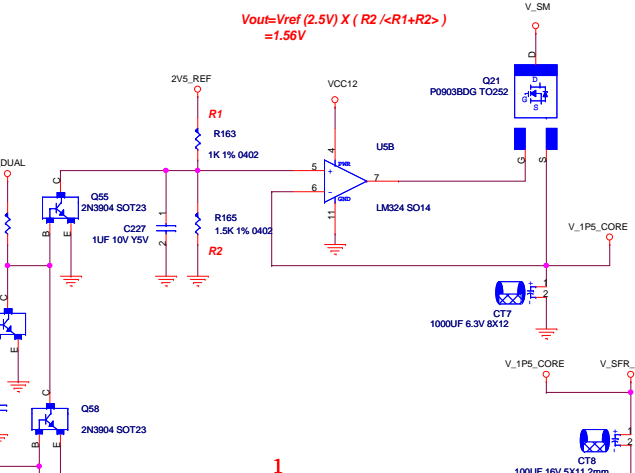
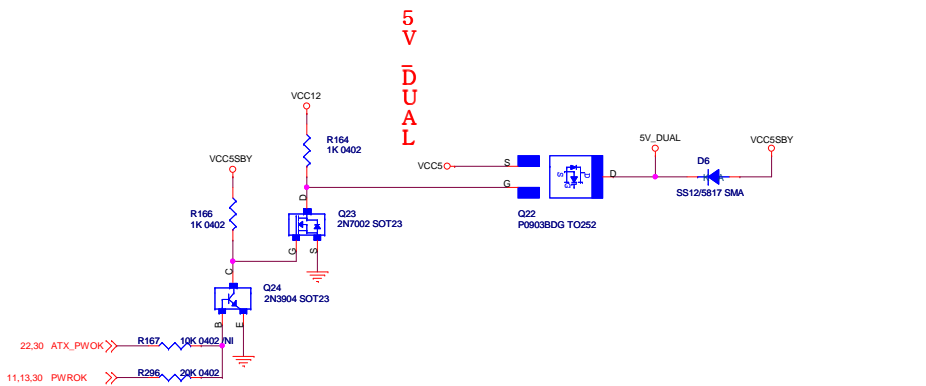
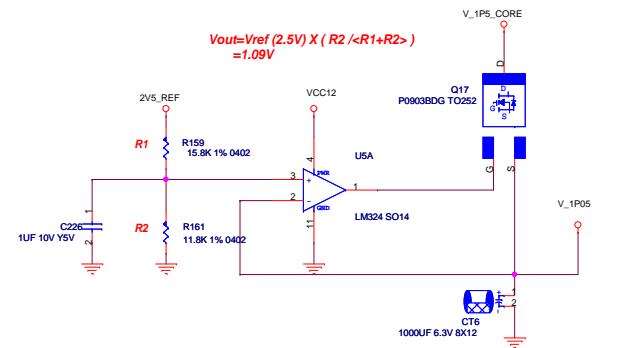
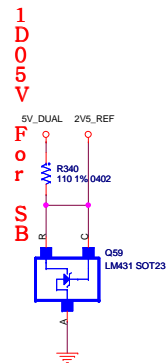
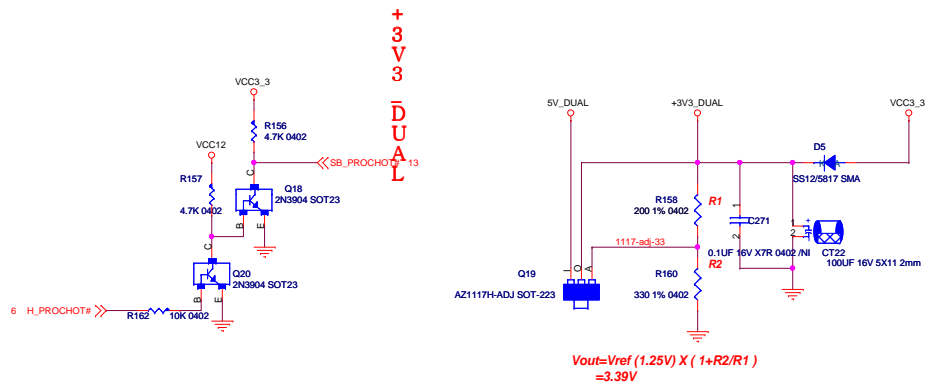


UP6206 FOR Intel P4 VRD11.1 POWER CKT - 4 PHASE

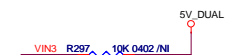
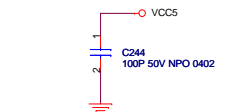
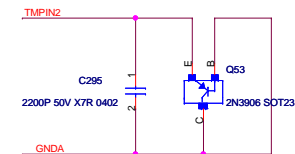
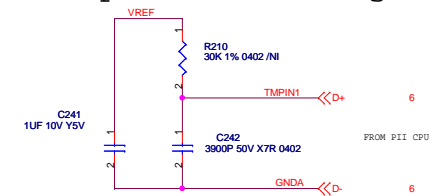
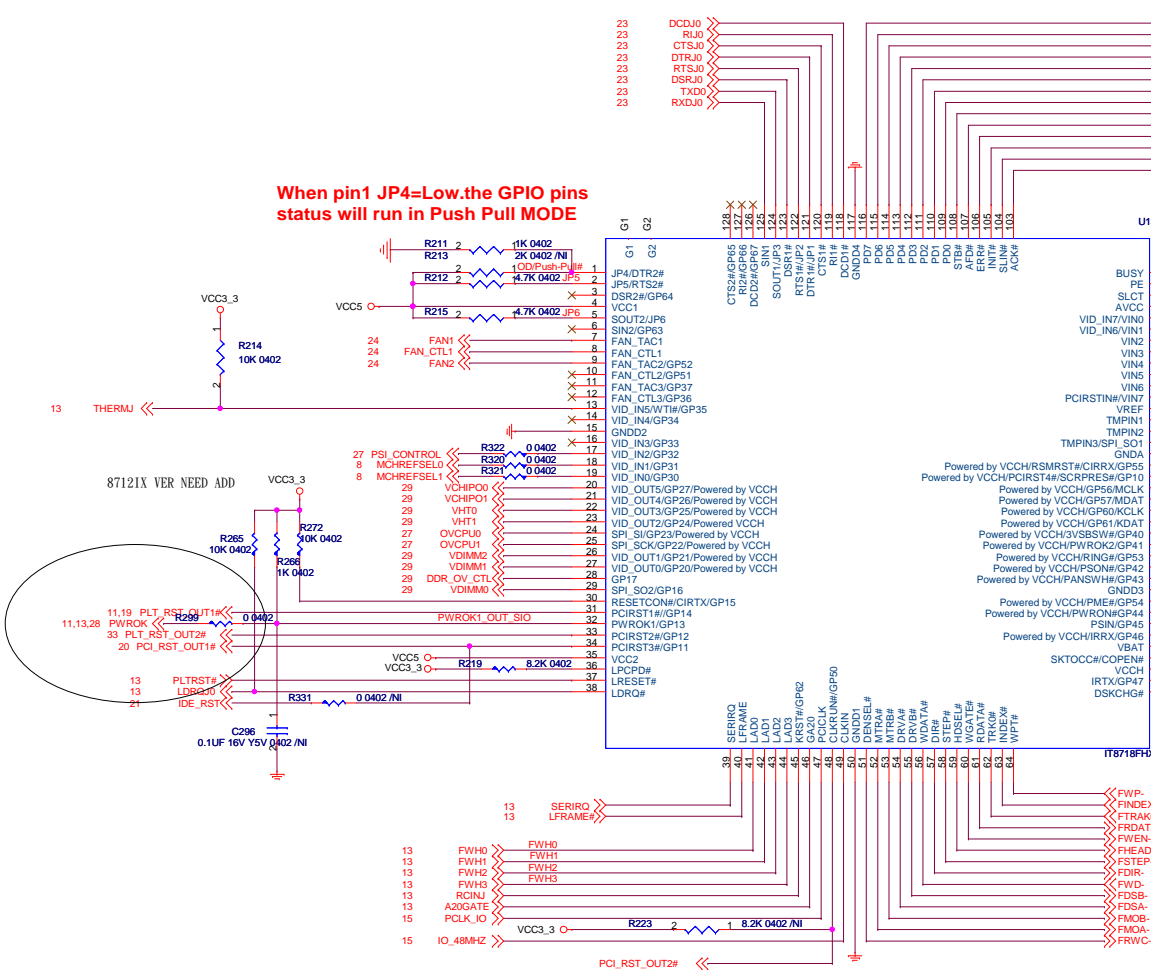


- 1.  $P_{osi} V_{ofs} = 0.4 / R_{ofs} * R_{fb}$
- 2.  $Nega V_{ofs} = 1.6 / R_{ofs} * R_{fb}$
- 3.  $P_{S} = 10000 / R_{rt}$
- 4.  $OCP I_{avg} = I_{out} * DCR / R_{csn}$   
 $OCP 60\mu A = I_{out} * DCR / R_{csn}$
- 5.  $P * L / DCR = RCSP * C_{cs}$

PSI_CONTROL	PSI
H	OPEN
L	CLOSE



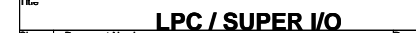


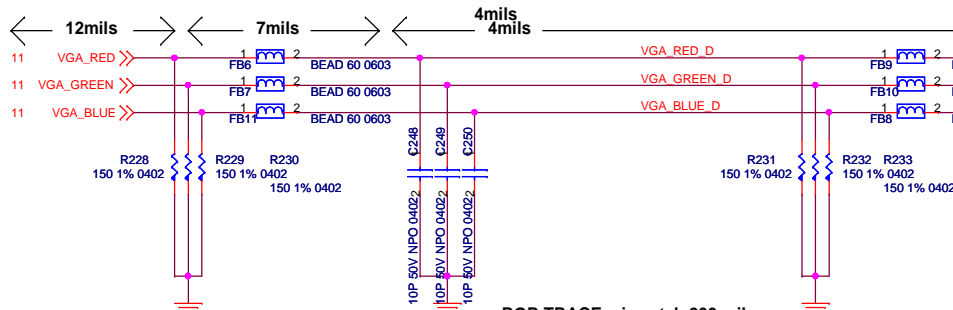
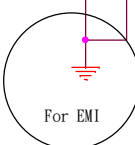
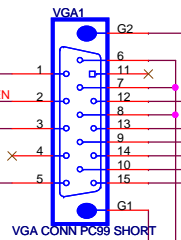
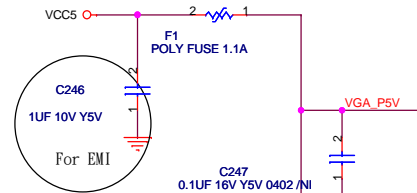
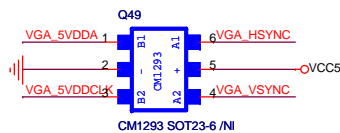
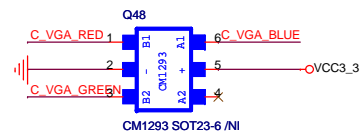


The schematic diagram illustrates the power supply section of the V1 IP1 CORE. It shows the connection of various power pins to the board. The input voltages are 1.0V, 3.3V, 12V, 5V, and 1.5V respectively. The diagram includes resistors (R311, R312, R313, R222, R224, R225) and capacitors (C286, C287, C288, C289, C290, C291) for decoupling and filtering. The connections are as follows:

- CPU\_VCCP** (1.0V) is connected to **R311** (10K 1% 0402) and **C286** (0.1UF 16V Y5V 0402).
- VCC3.3** (3.3V) is connected to **R312** (10K 1% 0402) and **C287** (0.1UF 16V Y5V 0402).
- VCC12** (12V) is connected to **R313** (10K 1% 0402) and **C288** (0.1UF 16V Y5V 0402).
- V\_SM** (5V) is connected to **R222** (30K 1% 0402) and **C289** (0.1UF 16V Y5V 0402).
- V\_FSB\_VTT** (1.5V) is connected to **R224** (51 0402) and **C290** (0.1UF 16V Y5V 0402).
- V\_FSB\_VTT** (1.5V) is also connected to **R225** (10K 1% 0402) and **C291** (0.1UF 16V Y5V 0402).

The diagram also shows the connection of the **VIN0**, **VIN2**, **VIN4**, and **VIN6** pins to the board. The **VIN0** and **VIN2** pins are connected to the **VCC3.3** pin. The **VIN4** and **VIN6** pins are connected to the **VCC12** pin.

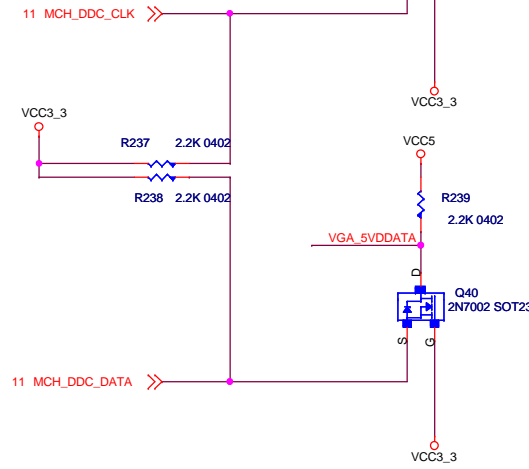
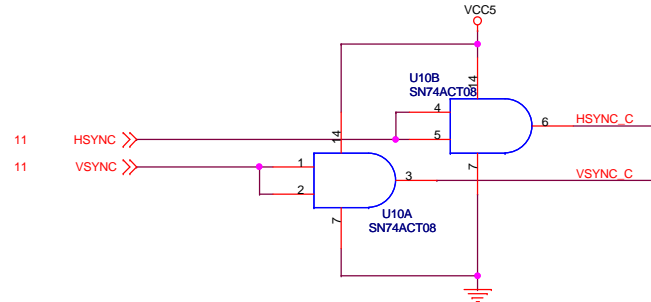
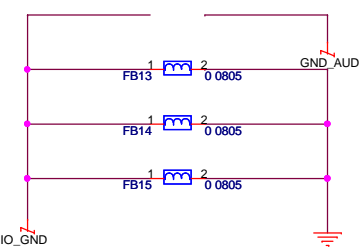




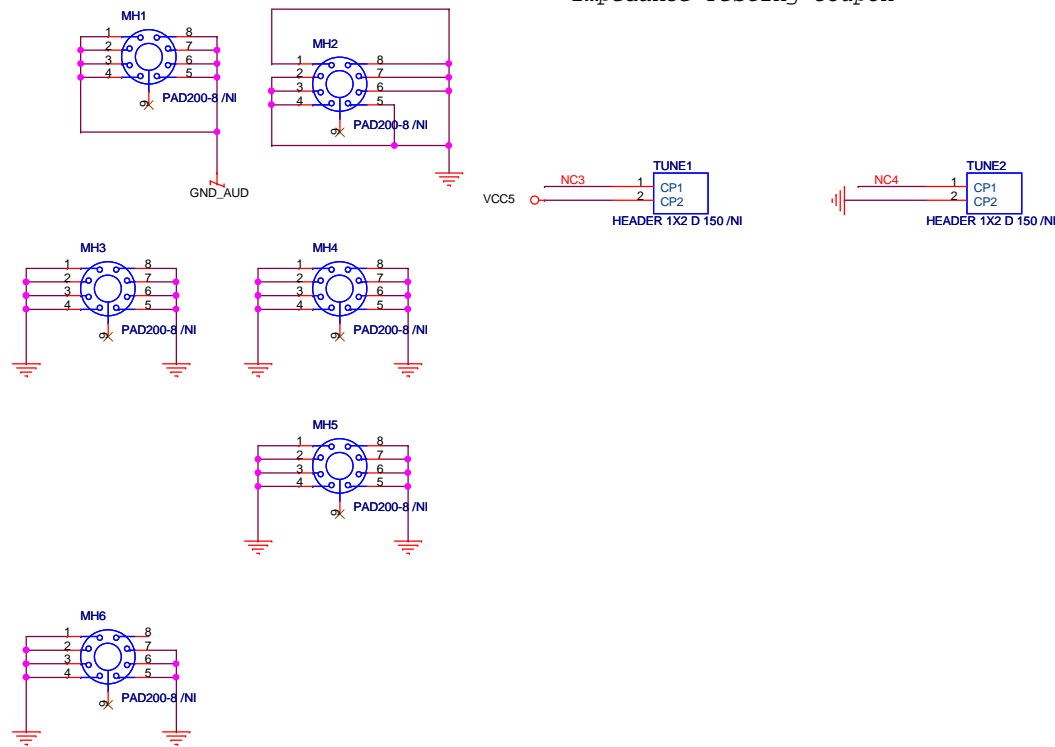
RGB TRACE mismatch 200 mils

chipset breakout 12mils to first R less 500mils, 1R to 2R route 7 mils, after 2R all 4 mils

R close GMCH less 500mils



# Impedance Testing Coupon







JUSBV1(2\_3)  
JUMPER 2P R

JUSBV2(2\_3)  
JUMPER 2P R

JCMOS1(1\_2)  
JUMPER 2P B

(Y1)  
X'TAL WIRE

New JPANEL1  
JPANEL1 2\*8

JPANEL1(9\_10) JPANEL1(15\_16)  
HEADER 1X2 HEADER 1X2  
JPANEL1(11\_14)  
PLED



JPANEL1(1\_4) JPANEL1(5\_6)JPANEL1(7\_8)  
SPK HLED RST

PCB  
IG41A-M7S V6.5

(PCB)  
泡棉  
POLON 235X182

(BAT1)  
電池  
3V BATTERY SONY

(U1)  
FLASH ROM  
SPI MX25L8005 DIP

(NB1)  
北橋散熱片  
SBLS-T

南橋散熱片  
(ICH1)  
BNP SMALL-L



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Title

BOM

Size  
A

Document Number

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Rev  
6.5

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